

VS10XX AppNote: Connecting analog outputs

Description

This document describes how to protect the analog outputs of VS10XX series devices from ESD and how to make a protected line-out connection. It shows an example schematic and gives general info on output protection including issues with single ended line-out connections.

This document applies to VS1001, VS1011, VS1002, VS1003 and VS1033.

Revision History			
Rev	Date	Author	Description
1.22	2006-08-18	PLe	Additional ESD protection and line-out info
1.21	2006-04-20	PLe	New Simple line-out schematic.
1.20	2006-04-06	PLe	Notes on power-down.
1.10	2006-03-06	PLe	More info on ESD.
1.00	2006-02-28	PLe	Initial revision.

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1 Background

VS10XX devices are qualified to withstand an ESD charge of 2 kV according to MIL-STD-883 method 3015.7 HumanBody Model (HBM). Additional protection is needed when VS10XX's analog outputs are connected to external connectors that may give higher energy electrical shocks than the HBM. An example would be earphones with long cable, where up to 15 kV ESD pulses need to be treated.

1.1 What is ESD?

ESD (ElectroStatic Discharge) generally means the discharge of energy charged between two subjects. ESD is generated from two insulators or a conductor and an insulator rubbing together. Electrons transfer from one subject to the other and a charge is generated. For example, a person walking across a carpet floor can generate a static charge of over 10kV. Two most common ESD models used in IC testing are Human Body Model and Machine Model.

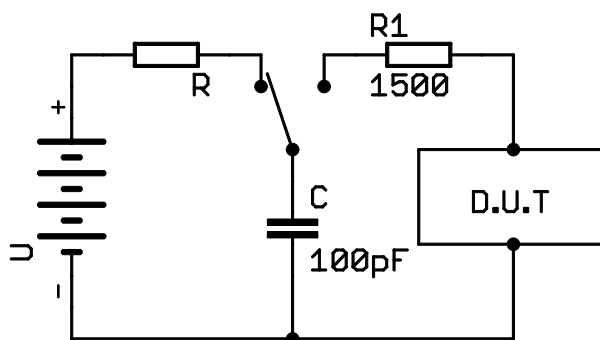


Figure 1: The Human Body Model (HBM)

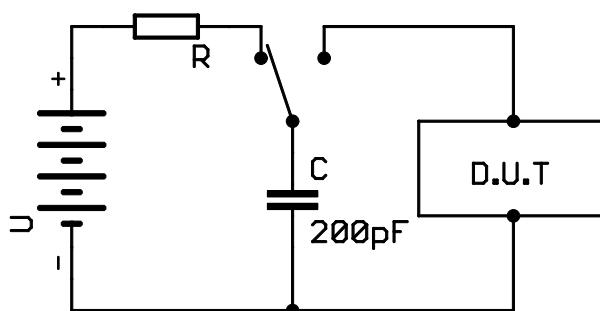


Figure 2: The Machine Model (MM)

The Human Body Model (HBM) replicates the typical discharge from the finger of a standing person of average weight and height. Testers use a 100pF capacitor in series with a 1500ohm resistor to simulate the ESD from people. (Figure 1)

Machine Model (MM) shown in figure 2 replicates the charge generated by for example “pick and place” IC handlers or soldering iron. The MM has no series resistance but a larger capacitor. The voltages in MM test are generally lower than in HBM. Due to the lack of the series resistor chips often fail in lower voltages than in HBM tests. (Reference: Carl Duffy, AMD, Test & Measurement Europe/April-May 1998)

Our qualification tests use the HBM. IC’s are tested (or “shot”) with three positive and three negative pulses between each pin. Ground pins are grouped together. Each pin is then tested against GND. Next each pin is tested against each power pin group. In last phase each IO pin is tested against any other IO pin.

2 Output Connection Using GBUF

In VS10XX devices the analog output pins (LEFT, RIGHT and GBUF) are biased close to 1.25V to allow DC-coupling to headphones. Minimal recommended output connection is shown in figure 3.

The RC-combo on each analog pin protects the VS10XX device from ESD surges on the analog signals. The RC-combo also provides a resistive load for the DAC at high frequencies and must not be omitted even if other methods of ESD protection are used.

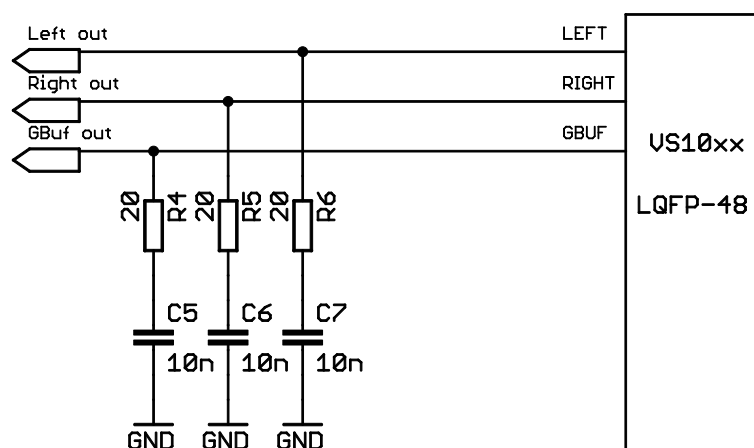


Figure 3: Minimal output connection using RC-protection

Laboratory tests show that this connection can tolerate 8kV ESD pulses (HBM) repeatedly with no damage to the VS10XX device. Depending on the application the system may halt or reset itself but the VS10XX device is not damaged. Tests were conducted with Prototyping board (http://www.vlsi.fi/player_vs10xx_proto/player.shtml) and ESD pulses were shot to the output connector with power on and with and without headphones.

To prevent ESD surges entering the PCB the RC-combo should be placed as close to the output connector as possible. High frequency capacitors with low internal resistance should be used.

2.1 Additional ESD Protection

Extra protection can be achieved by using a suitable TVS (Transient Voltage Suppressor). Figure 4 shows one way of connecting TVS to VS10XX. The TVS should be connected as close to the input connector as possible. Quality device with short turn-on time and suitable clamping voltage and peak pulse power should be selected.

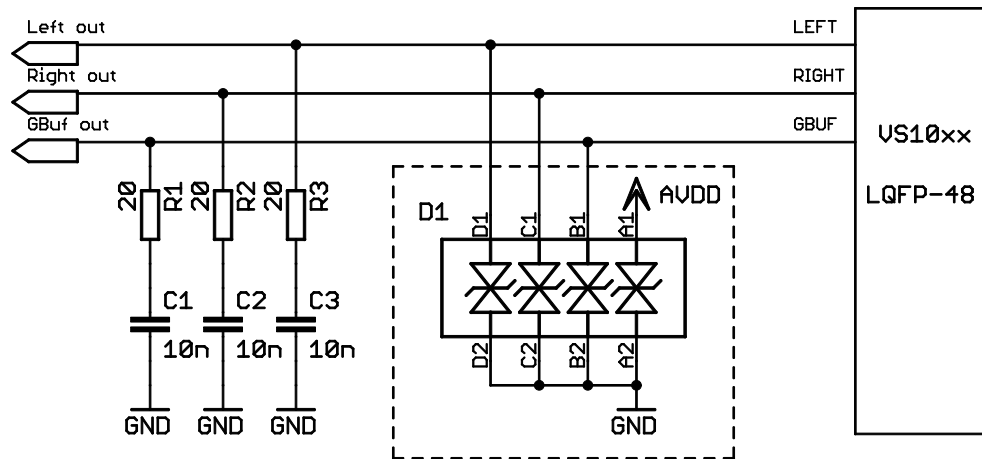


Figure 4: ESD protection using Transient Voltage Suppressor (TVS)

Our laboratory tests show that with a good TVS device VS10XX devices can tolerate ESD pulses (HBM) up to 10kV contact discharge and 16kV air discharge (HBM). Test setup was the same as with RC protection.

ESD protection diodes can also be used to provide extra protection. Figure 5 shows one way of using diodes to protect the analog signals. Notice C8 which provides a short path to GND for positive ESD surges when a short connection to AVDD is not possible.

Traces on PCB must be kept as short as possible to minimize parasitic inductances. Good grounding is essential. Ground plane should be used for best performance.

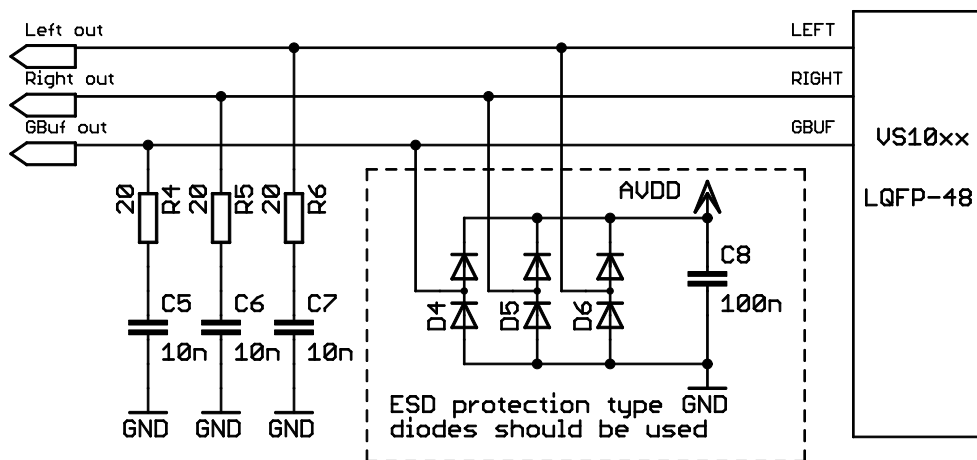


Figure 5: ESD protection using diodes

3 Line-out Connection

It's not recommended to use GBUF as audio ground when connecting to other electrical equipment such as power amplifiers or PC line-inputs. The GBUF pin is internally biased to 1.25V and it is possible that a ground loop is formed when the GBUF is connected to the ground of the target device. *This may damage the VS10XX device and will prevent normal operation.*

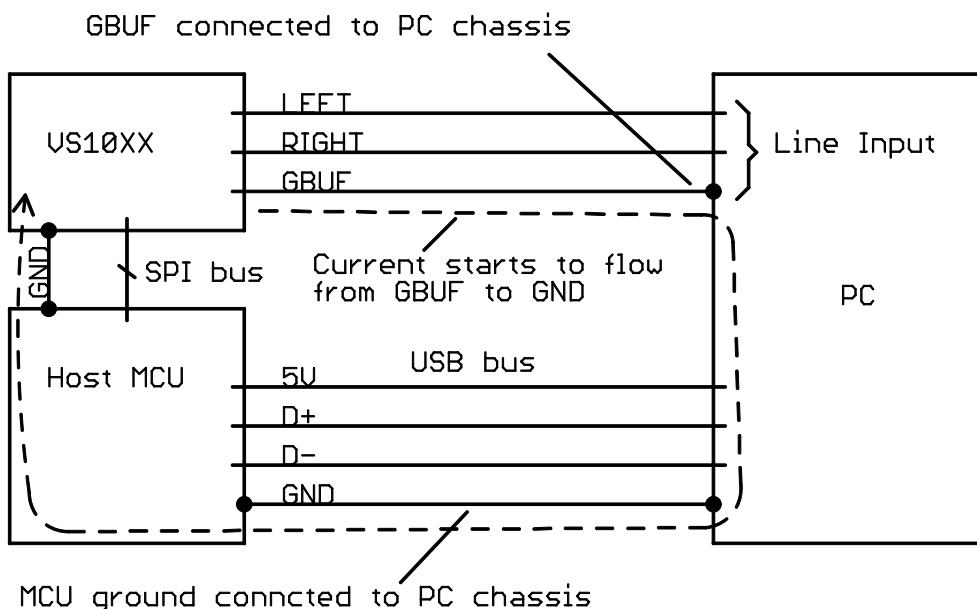


Figure 6: Ground loop is formed when GBUF and USB is connected to PC ground

A ground loop can happen for example with a VS10XX application that uses GBUF and has USB or Ethernet connected and the output of VS10XX is connected to a PC soundcard. Figure 6 illustrates this situation. DC blocking capacitors should be

used and the outputs referenced to ground.

Notice: **GBUF must not be connected to ground!**

3.1 Recommended Connection

A power-on transient is a general problem of any single-ended audio device. Since the analog outputs are biased above zero there will be a pop when the coupling capacitors charge during power-up. This chapter shows a way to minimize this transient.

Figure 7 shows the current recommendation for a high quality line-out. It uses an analog switch to isolate the output pins during boot-up. The coupling capacitors C1 and C2 charge slowly through R5 and R6 when the switches are open. When caps are fully charged the switches are closed and outputs are enabled.

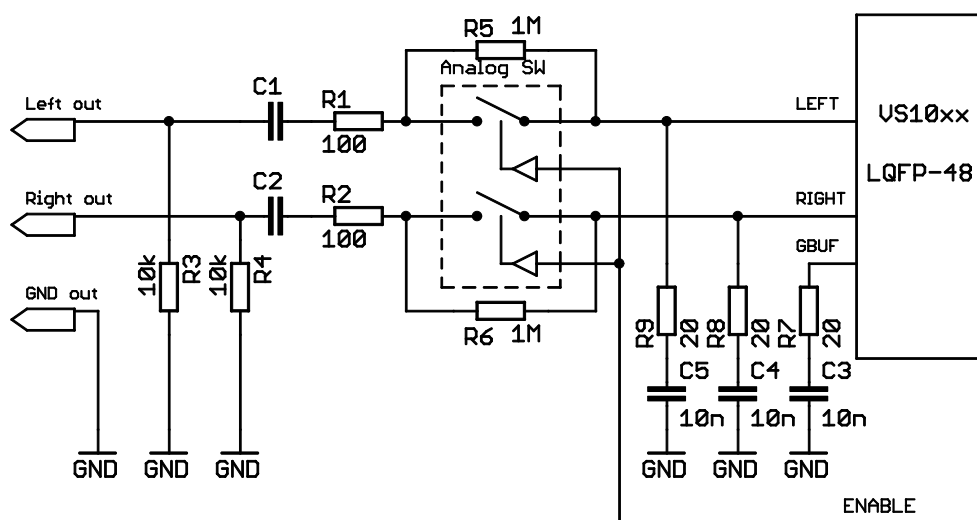


Figure 7: Transient free line-out connection

Notice that the ESD protection described in the previous chapter must also be used with the line-out connection. ESD components should be placed after the line-out components and as close to the output connector as possible. Additional protection may be needed for the analog switch.

The analog SW and R5 and R6 can be omitted if a power-on click is not an issue in the application.

The value of C1 and C2 should be chosen based on the input impedance of the amplifier the VS10XX will be connected to and on the low freq cut-off desired.

The cut off frequency is calculated as follows: $f_{-3dB} = \frac{1}{2\pi RC}$ where: $C = C1$
 $R = R1 + \frac{R3 * R_{load}}{R3 + R_{load}}$ and R_{load} is the resistance of the load. Bigger C will give lower

cut-off frequency but increases required wait time to enable the analog switches.

Usage (power-up):

1. Keep VS10XX in reset
2. Use uC to turn ENABLE off (open switches)
3. Release VS10XX from reset (set XRESET high)
4. Wait for 100ms
5. Turn ENABLE on (close switches)

If there is still a pop when outputs are enabled, wait a bit longer.

Usage (power-down):

1. Put VS10XX to analog powerdown (set SCI_VOL register to 0xFFFF)
2. Turn ENABLE off (open switches)
3. Put VS10XX to reset (set XRESET low)

3.2 Simple Connection

Figure 8 shows the current recommendation for a simplified line-out connection. This connection is suitable for example when connecting VS10XX to an external on-board amplifier.

Some transient in the outputs during power up and down will occur if the startup is not slowed down with software.

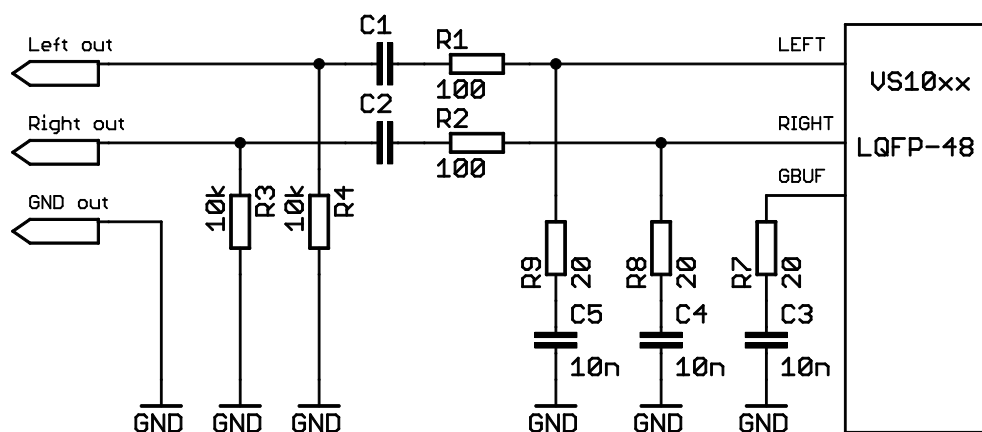


Figure 8: Simple line-out connection

4 Document Version Changes

This chapter describes the most important changes to this document.

Version 1.22, 2006-08-18

- Updated ESD protection recommendations. Added TVS info. Added info on line out.

Version 1.21, 2006-04-20

- Updates to line-out schematic and a new simplified line-out connection.

Version 1.20, 2006-04-06

- Notes on power-down.

Version 1.10, 2006-03-06

- More detailed ESD info added.

Version 1.00, 2006-02-28

- Initial version.

5 Contact Information

VLSI Solution Oy
Hermiankatu 8 B
FIN-33720 Tampere
FINLAND

Phone: +358-3-340 8222

Email: mp3@vlsi.fi

URL: <http://www.vlsi.fi/>

Note: If you have questions, first see

<http://www.vlsi.fi/vs1001/faq/>

<http://www.vlsi.fi/vs1011/faq/>

<http://www.vlsi.fi/vs1002/faq/>

<http://www.vlsi.fi/vs1003/faq/>

<http://www.vlsi.fi/appnotes/>