MA8201

MP3 Decoder & DAC Controller

User's Manual

V1.0

MosArt

SEMICONDUCTOR CORP.

Features

- MPEG audio layer 1, 2, and 3 decoder (ISO 11172-3)
- Supports MPEG 1 & 2 for all layers, and Layer 3's 2.5 extensions, and all their sample rates and bit-rates, in mono or stereo
- PCM input mode
- Supports VBR (variable bit-rate) for MP3
- Can be used as a slave co-processor
- Operates with single clock 12.288..16 MHz or 24.576..32 MHz.
- Extremely low-power operation
- On-chip high-quality stereo DAC with no phase error between channels
- Internal Op-Amp
- Stereo earphone driver capable of driving a 30- load.
- Separate 2.5 .. 3.6V operating voltages for analog and digital
- Serial control and data interfaces
- New functions may be added with software

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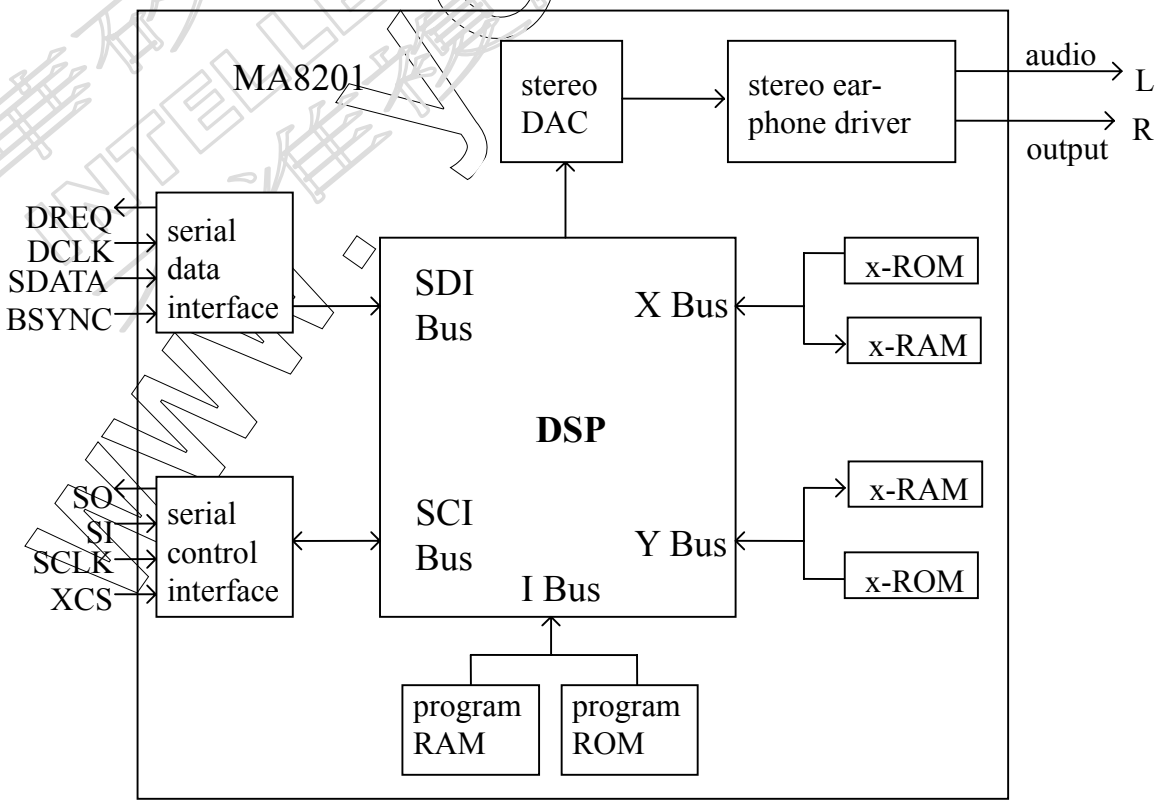
Description

MA8201 is a single-chip solution for an MPEG layer 1, 2 and 3 audio decoder. The chip contains a high-performance low-power DSP processor core (MosArt DSP), working memory, user applications, serial control and input data interfaces, and a high-quality over sampling variable sample-rate stereo DAC, followed by an earphone amplifier and a ground buffer. MA8201 receives its input bit-stream through a serial input bus, which it listens to as a system slave. The input stream is decoded and passed through a analog/digital hybrid volume control to an 18-bit over sampling, multi-bit, sigma-delta DAC. The decoding is controlled via a serial control bus.



1 Description

MA8201 is a single-chip solution for an MPEG Layer 1, 2 and 3 audio decoder. Which is a LQFP 44 package. It's suitable for small and low power portable audio device.

2 Characteristics & Specifications

Unless otherwise noted: AVDD=2.7V, DVDD=2.5V, TA=+25±C, XTALI=24.576MHz, Full-Scale Output Sine wave at 1.125 kHz, measurement bandwidth 20..20000 Hz, bit-stream 128kbits/s, local components as shown in Figures 4 and 5.

2.1 Analog Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
DAC Resolution			16		Bits
DAC Differential No linearity	DNL			±0.9	LSB
Total Harmonic Distortion	THD		0.1	0.2	
Dynamic Range (DAC unmated, A-weighted)	IDR	85	90		dB
S/N Ratio	SNR		87		dB
Inter channel Isolation		60	75		dB
Gain Error				0.1	dB
Inter channel Gain Mismatch				0.2	dB
Frequency Response		-0.1		0.1	dB
Full Scale Output Voltage (Peak-to-peak)			1.8[1]		Vpp
Gain Drift			100		ppm/^{0}C
Deviation from Linear Phase				5	^{0}
Out of Band Energy			-60		dB
Out of Band Energy with Analog Filter			-90		dB
Analog Output Load Resistance		10	30		Ω
Analog Output Load Capacitance				1000	pF
Power Supply Rejection			40		dB
Power Supply Consumption AVDD, Reset			0.1	1.0	μA
Power Supply Consumption AVDD, no load		3.0	4.5	6.0	mA
Power Supply Consumption AVDD, output loaded at 30Ω		4.0	5.5	40.0	mA
Power Supply Consumption AVDD, o. @ 30Ω+ GND-buf.		6.0	7.5	40.0	mA
Power Supply Consumption DVDD, Reset			0.5	2.0	μA
Power Supply Consumption DVDD			15.0		mA

1 3.6 volts can be achieved with +-to-+ wiring for mono sound.

2.2 DAC Interpolation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Pass band (to -3dB corner)		0		0.459Fs	Hz
Pass band (Ripple Spec)		0		0.420Fs	Hz
Pass band Ripple				±0.0.56	dB
Transition Band		0.420Fs		0.580Fs	Hz
Stop Band		0.580Fs			Hz
Stop Band Rejection		90			dB
Group Delay			15/Fs		s

Fs is conversion frequency

2.3 DAC Interpolation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
-3 dB bandwidth		300			kHz
Pass band Response at 20 kHz		-0.05			dB

2.4 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Analog Positive Supply	AVDD	-0.3	3.6	V
Digital Positive Supply	DVDD	-0.3	3.6	V
Current at Any Digital Output			±50	mA
Voltage at Any Digital Input		DGND-1.0	DVCC+1.0	V
Ambient Operating Temperature (power applied)		-20	80	^{0}C
Storage Temperature		-65	150	^{0}C

2.5 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Analog and Digital Ground	AGND DGND		0.0		V
Positive Analog (Functional)	AVDD	2.5	3.0	3.6	V
Positive Analog (In Spec)	AVDD	2.7	3.0	3.6	V
Ambient Operating Temperature		0		7.0	^{0}C

The following values are to be used when the clock doubler is active:

Parameter	Symbol	Min	Typ	Max	Unit
Positive Digital	DVDD	2.5	2.7	3.6	V
Input Clock Frequency	CLKF		12.288	13	MHz
Internal Clock Frequency[1]	CLKI		24.576	26	MHz

1 The maximum sample rate that may be decoded with correct speed is CLKI/512.

The following values are to be used when the clock doublers is inactive:

Parameter	Symbol	Min	Typ	Max	Unit
Positive Digital	DVDD	2.5	2.7	3.6	V
Input Clock Frequency	CLKF		24.576	26	MHz
Internal Clock Frequency[1]	CLKI		24.576	26	MHz

1 The maximum sample rate that may be decoded with correct speed is CLKI/512.

Note: With higher than typical voltages, MA8201 may operate with CLKI up to 30..32 MHz. However, the chips are not qualified for this kind of usage. If necessary, MosArt can qualify chips for higher clock rates for quantity orders.

2.6 Digital Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage			2.25		V
Low-Level Input Voltage				0.8	V
High-Level Input Voltage at I*o* = -2.0 mA		0.9DVDD			V
Low-Level Output Voltage at I*o* = -2.0 mA				0.1DVDD	V
Input Leakage Current				1.0	μA

2.7 Switching Characteristics - Clocks

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frecquency[1]	XTALI		12.288		MHz
Master Clock Frecquency[2]	XTALI				MHz
Master Clock Duty Cycle		40	50	60	%
Clock Output	XTALO		XTALI		MHz

[1] Clock doublers active.

[2] Clock doublers inactive.

2.8 Switching Characteristics - DREQ Signal

Parameter	Symbol	Min	Typ	Max	Unit
Data Request Signal	DREQ			200	ns

2.9 Switching Characteristics - SPI Interface Output

Parameter	Symbol	Min	Typ	Max	Unit
SPI Input Clock Frequency				0.25×CLKI	MHz
Rise timer for SO				100	ns

2.10 Switching Characteristics - Boot Initialization

Parameter	Symbol	Min	Max	Unit
-RESET active time		2		clocks
-RESET inactive to software ready			50000	clocks

2.11 Short-Circuiting Analog Outputs

Although not a recommended practice for prolonged times, short-circuiting analog outputs and/or ground does not cause physical harm to the chip. Nevertheless, if using an earphone connection, high electrical charges may harm MA8201's analog outputs.

2.12 Using an External Clock

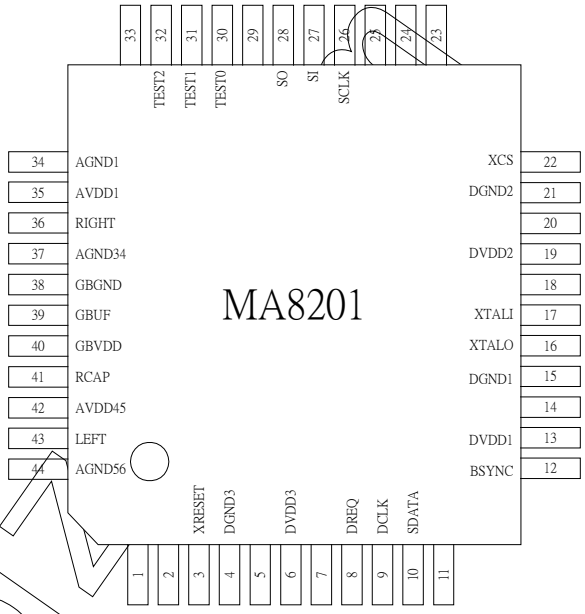
If there is a pulse or sine clock signal available from some other device, it may be connected to pin XTALI. In this case, leave XTALO unconnected, i.e. floating. Note, that unless the clock is stopped while reset is active, reset power consumption may be radically different from what is presented in Chapter 2.1. Note also that when the chip is in hardware reset, XTALO and XTALI are grounded. Thus, if there is an external clock that doesn't go to ground when MA8201 is reset, you should use safety resistors between the clock source and XTALO and XTALI.

3 Package & Pin Discriptions

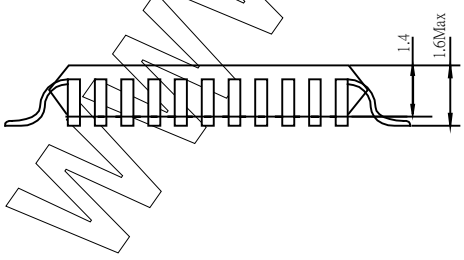
3.1 LQFP-44

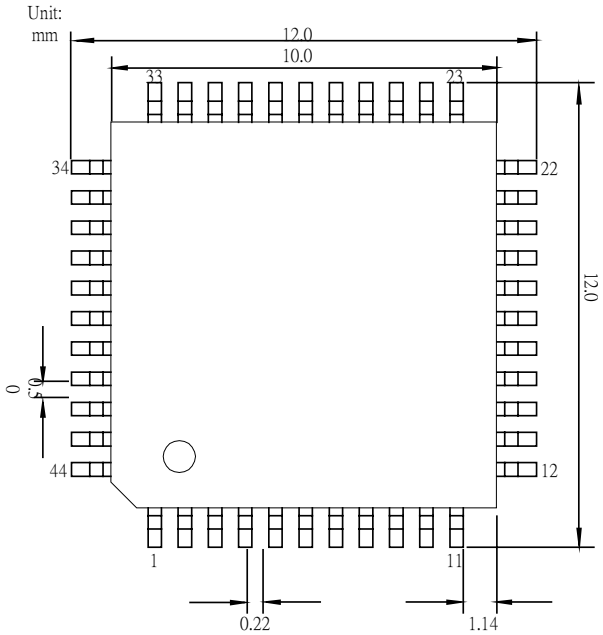
Pin types:

- DI = digital input, CMOS Input Pad
- DO = digital output, CMOS Input Pad
- DIO = digital input/output
- DO3 = digital output, CMOS Tri-stated Output Pad
- AO = analog output
- CLK = clock/crystal connection
- PWR = power supply pin



3.2 Package





3.3 Pin Discriptions

Pin Name	Pin	Type	Function
XRESET	3	D1	active low asynchronous reset
DGND3	4	PWR	digital ground
	5		
DVDD3	6	PWR	digital power supply
	7		
DREQ	8	DO	data request. input bus
DCLK	9	DIO	serial input data bus clock
SDATA	10	DI	serial data input
	11		
BSYNC	12	DI	byte synchronization signal
DVDD1	13	PWR	Digital power supply
	14		
DGND1	15	PWR	Digital ground
XTAL0	16	CLK	Crystal output
XTALI	17	CLK	Crystal input
	18		
DVDD2	19	PWR	Digital power supply
	20		
DGND2	21	PWR	Digital ground
XCS	22	DI	Chip select input(active low)
	23		
	24		
	25		
SCLK	26	DI	Clock for serial bus
SI	27	DI	Serial input
SO	28	DO3	Serial output
	29		
TEST0	30	DI	Reserved for test, connect to DVDD
TEST1	31	DIO	Reserved for test, do NOT connect
TEST2	32	DIO	Reserved for test, do NOT connect
	33		
AGND1	34	PWR	Analog ground
AVDD1	35	PWR	Analog power supply
RIGHT	36	AO	Right channel output
AGND34	37	PWR	Analog ground
GBGND	38	PWR	Analog ground for ground buffer
GBUF	39	PWR	Ground buffer
GBVDD	40	PWR	Analog power supply for ground buffer
RCAP	41	AIO	Capacitance for reference
AVDD45	42	PWR	Analog power supply
LEFT	43	AO	Left channel output
AGND56	44	PWR	Analog ground

For pin types, look at Chapter 3.1.

4 Connection Diagram, LQFP-44

In this connection diagram, a LQFP-44 -packaged MA8201 is used. In this picture, ground buffer is active.

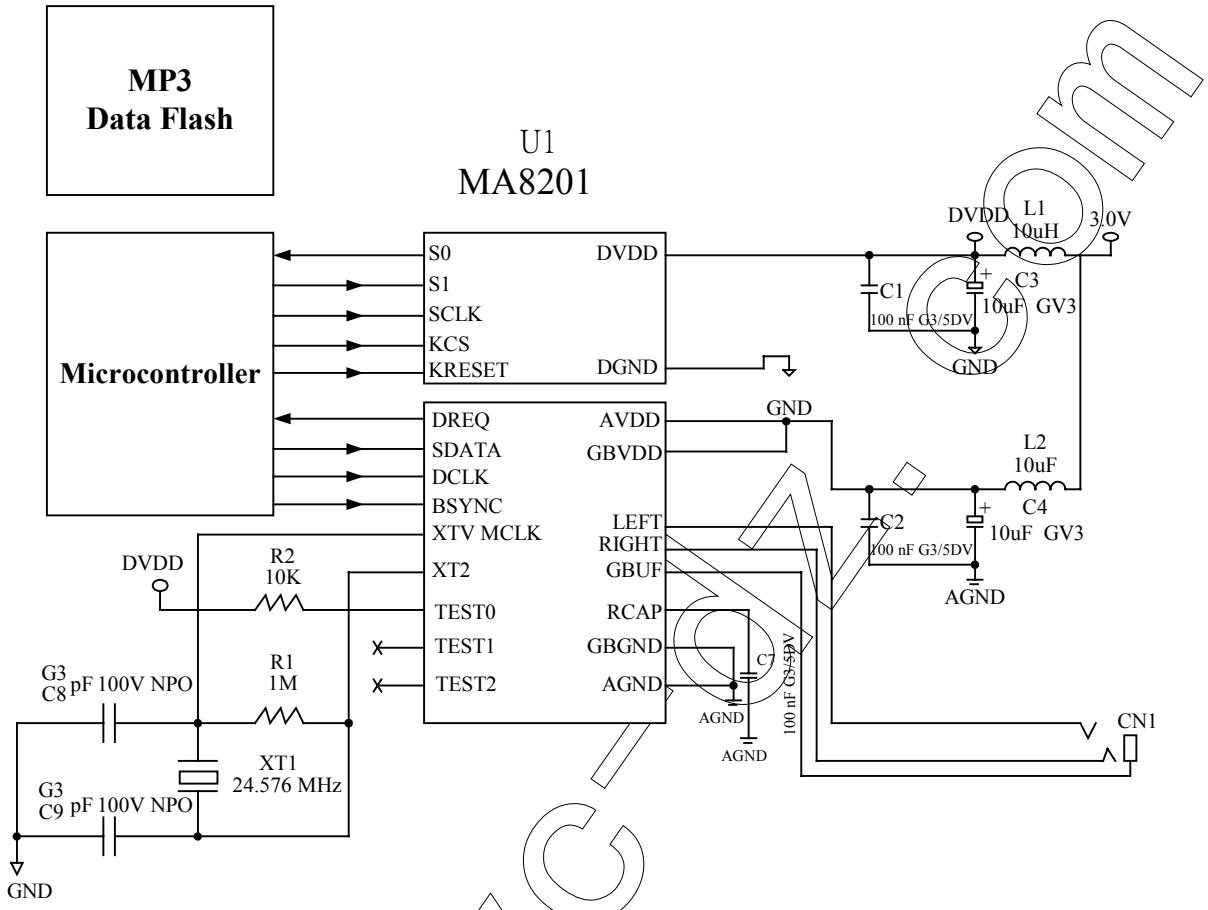


Figure 5: Typical Connection Diagram

Ground buffer GBUF can be used for common voltage (1.37 V) for earphones. This will eliminate the need for large isolation capacitors on line outputs, and thus the audio output pins fromMA8201 may be connected directly to the earphone connector. If GBUF is not used, GBGND and GBVDD should not be connected.