MA8201-H72

8-bit USB Mass Storage with MP3 Decode Embedded Processor

User's Manual

V2.7

MosArt

SEMICONDUCTOR CORP.

Content

1. INTRODUCTION

The 8-bit embedded processor is designed for a high performance, low-cost and cost-effective general-purpose system.

By providing 3.3V, fully static operation in an efficient package, the MA8201-H72 delivers cost-effective performance to satisfy the extensive requirements.

The MA8201-H72 (shown in Figure 1) is the highly integrated processor of MA8000 CPU inside. MA8000 CPU is 8-bit CISC architecture, low-power, simple, full static design and powerful instruction set is suitable for cost-effective and power sensitive applications.

To reduce total system cost, the embedded processor includes a RC oscillator, a phase locked loop synthesis clock, two set of programmable timers, a serial peripheral interface, a clock timer, a IIS interface, a CODEC decode and a USB controller.

The chip support MPEG1/MPEG2, layer 3 format.

MP3 support sampling rate : 16K/22.05K/24K/32K/44.1K/48K.

MP3 support bit rate : 32K ~ 320K, VBR also support.

1.1 KEY FEATURES

To provide a complete set of general system peripherals, the MA8201-H72 reduces overall system costs and configure additional components. The primary features are as follows:

Incorporates Many Functions Typically Relegated to External Array Logic, such as:
System Configuration, Programmable Address Mapping

- ✧ 8-bit MA8000 core CPU compatible with WDC 6502 core
- ✧ On-chip clock generator 48MHz and 32KHz
- ✧ Phase Locked Loop clock synthesis
- ✧ NAND Flash memory interface
- ✧ Two 16-bit programmable timers
- ✧ Clock timer
- ✧ Serial peripheral interface
- ✧ USB 1.1 device controller
- ✧ MP3/ADPCM/PCM decode
- ✧ IIS interface
- ✧ UART interface

● **Built-in Low Frequency RC Oscillator**

Low frequency oscillator (about 32 KHz) for power saving mode

● **Phase Locked Loop Clock Synthesis**

Large Scale about Synthesis Range (32KHz -> 16MHz)

Low Current Consumption (< 1.5 mA)

Flexible Clock Rate by Software Programmable

● **Input Port**

Programmable Rising or Falling Interrupt

Built-in Pull-up or Pull-down Resistors

● **Programmable Timer**

16-bit programmable

Flexible Clock Source by Software Programmable

Automatic Interrupt Generation

- **Clock Timer**
  - Periodic Interrupt (About 1Hz, 2Hz, 4Hz, 8Hz, 16Hz, 32Hz, 64Hz)
  - RC oscillator clock operation
  - Automatic Interrupt Generation

- **Serial Peripheral Interface**
  - Supports 8/16/24/32-bit data transfer
  - Flexible Clock Source by Software Programmable
  - Automatic Interrupt Generation

- **NAND Flash Memory Controller**
  - Flexible clock rate by soft programmable
  - Automatic Interrupt Generation
  - ECC generation and check

- **Universal Serial Bus(USB) Interface**
  - Bulk Only Transfer Protocol
  - On-chip USB transceiver
  - Data Transfer Rate up to 1.2 MB/s

- **MP3/ADPCM/PCM Decode**
  - With data buffer
  - Adjustable 32 steps volume control
  - 10 bands equalizers
  - PCM or ADPCM encode/decode with 8K, 16K, and 32K sample
  - Automatic Interrupt Generation

- **IIS Interface**
  - Flexible clock rate automatically

- **UART Interface**
  - Supports Parity Check Bit
  - Supports 5/6/7/8/9/10/11/16-bit data transfer
  - Flexible clock rate by soft programmable
  - Automatic Interrupt Generation

- **Miscellaneous function**

  A 16x16 unsigned multiplication

  A 32/16 unsigned divider

  A parity checker

  A data rearrangement module

- **Interrupt Process Unit**

  Provide Interrupt Vector and Data

  Interrupt Priority Control and Selection

- **Power Management**

  Fully Static HCMOS Technology

  Programmable Clock Synthesizer for Full Frequency Control

  Low Power Stop Capabilities

  Modules Can Be Individually Shut-down

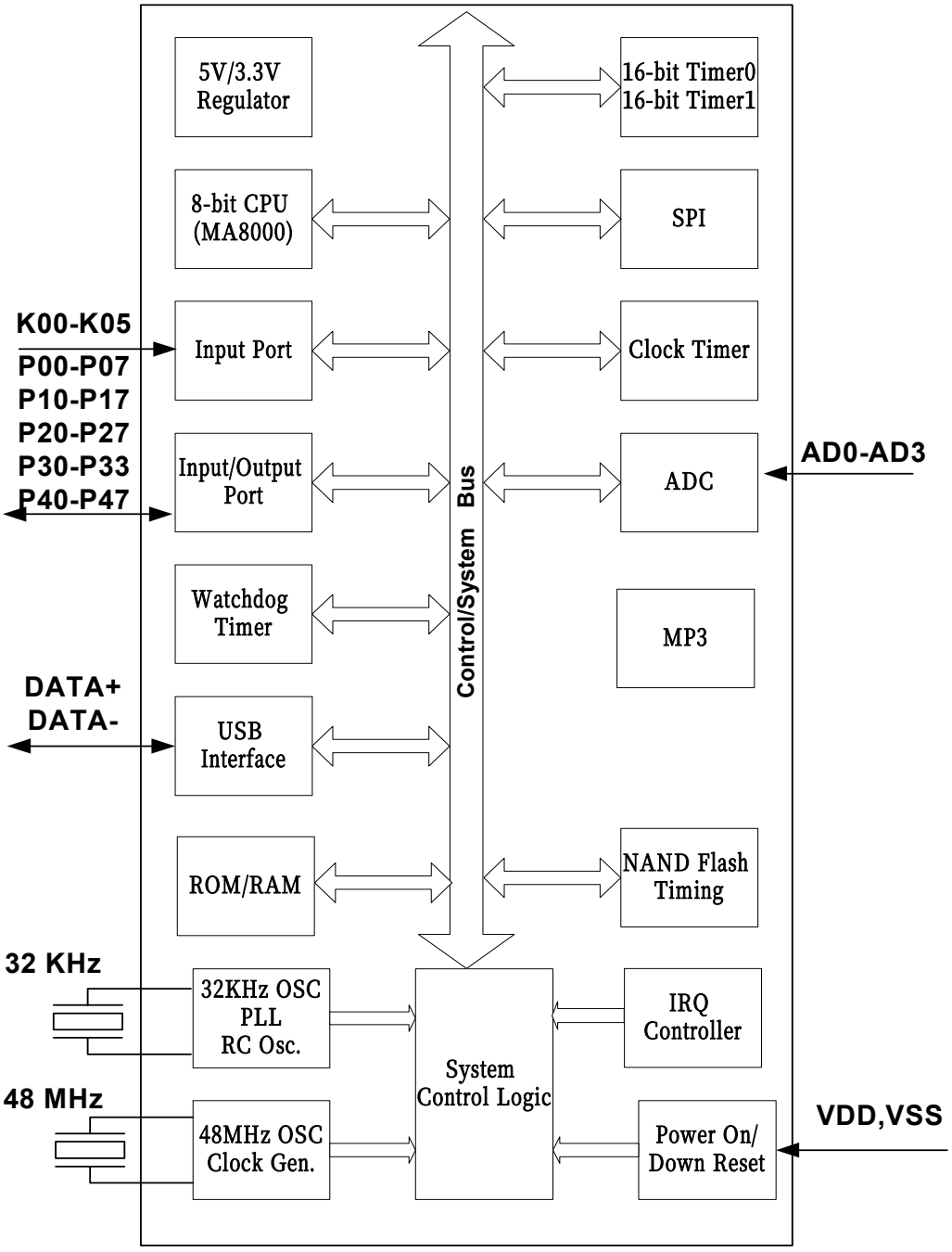
  Lowest Power Mode Control (Shut Down CPU and Peripherals)

- **Operation From DC To 24 MHz (Processor Clock)**

- **Operating Voltages of 2.7V ~ 3.6V**

- **Compact 64 LQFP Package**

1.2 BLOCK DIAGRAM



1.3 PIN LAYOUT DIAGRAM

PIN #	Pin Name	Input/Output	Pin Description	LQFP-64
1	XCLKI	Input	Crystal 48MHz Input	2
2	XCLKO	Output	Crystal 48MHz Output	3
3	XOSCI	Input	Crystal 32KHz Input	4
4	XOSCO	Output	Crystal 32KHz Output	5
5	CAP	Analog	External capacitor pin for PLL circuit	6
6	USB-	I/O	USB pin	10
7	USB+	I/O	USB pin	11
8	XRESET	Input	System reset input	31
9	K00	Input	I/O pin with software selectable	-
10	K01/SMXCD	Input	I/O pin with software selectable	23
11	K02/SDXCD	Input	I/O pin with software selectable	30
12	K03/RB	Input	I/O pin with software selectable	13
13	K04	Input	I/O pin with software selectable	32
14	K05	Input	I/O pin with software selectable	33
15	P00/D0/SDIO0	I/O	I/O pin with software selectable	35
16	P01/D1/SDIO1	I/O	I/O pin with software selectable	36
17	P02/D2/SDIO2	I/O	I/O pin with software selectable	37
18	P03/D3/SDIO3	I/O	I/O pin with software selectable	38
19	P04/D4/SDCMD	I/O	I/O pin with software selectable	39
20	P05/D5	I/O	I/O pin with software selectable	42
21	P06/D6	I/O	I/O pin with software selectable	43
22	P07/D7	I/O	I/O pin with software selectable	44
23	P10/CLE	I/O	I/O pin with software selectable	45
24	P11/ALE	I/O	I/O pin with software selectable	46
25	P12	I/O	I/O pin with software selectable	52
26	P13	I/O	I/O pin with software selectable	53
27	P14/XRE	I/O	I/O pin with software selectable	47
28	P15/XWE	I/O	I/O pin with software selectable	48
29	P16/XCE0	I/O	I/O pin with software selectable	18
30	P17/XCE1	I/O	I/O pin with software selectable	19
31	P20/SDCLK	I/O	I/O pin with software selectable	54
32	P21/XCE2	I/O	I/O pin with software selectable	20
33	P22/XCE3	I/O	I/O pin with software selectable	21
34	P23/XCE4	I/O	I/O pin with software selectable	22
35	P24/XCE5	I/O	I/O pin with software selectable	49
36	P25	I/O	I/O pin with software selectable	15
37	P26	I/O	I/O pin with software selectable	55
38	P27	I/O	I/O pin with software selectable	16
39	P30/SPIDI/XCE6	I/O	I/O pin with software selectable	50
40	P31/SPIDO/DATA	I/O	I/O pin with software selectable	51
41	P32/SPICK/BCK	I/O	I/O pin with software selectable	56
42	P33/SPIRDY/WS	I/O	I/O pin with software selectable	17
43	VPP	Power	Power pin (6.5V)	57

44	VDD	Power	Power pin (3.3V)	8,9,40
45	VSS	Power	Power pin (gnd)	1,12,41
46	AD0	Analog	ADC input	63
47	AD1	Analog	ADC input	62
48	AD2	Analog	ADC input	61
49	AD3	Analog	ADC input	60
50	VREF	Analog	ADC & OP power input	7
51	AVSS	Analog	ADC & OP power input	64
52	TXD	Output	UART transmit signal	58
53	RXD	Input	UART receive signal	59
54	P40	I/O	I/O pin with software selectable	14
55	P41	I/O	I/O pin with software selectable	24
56	P42	I/O	I/O pin with software selectable	25
57	P43	I/O	I/O pin with software selectable	26
58	P44	I/O	I/O pin with software selectable	27
59	P45	I/O	I/O pin with software selectable	28
60	P46	I/O	I/O pin with software selectable	29
61	P47	I/O	I/O pin with software selectable	34
62	VOL_L	Analog	Left volume adjust pin	61
63	VOL_R	Analog	Right volume adjust pin	60
64	NMIB	Input	MA8000 interrupt signal	-
65	A0	Output	MA8000 address output A0	-
66	A1	Output	MA8000 address output A1	-
67	A2	Output	MA8000 address output A2	-
68	A3	Output	MA8000 address output A3	-
69	A4	Output	MA8000 address output A4	-
70	A5	Output	MA8000 address output A5	-
71	A6	Output	MA8000 address output A6	-
72	A7	Output	MA8000 address output A7	-
73	A8	Output	MA8000 address output A8	-
74	A9	Output	MA8000 address output A9	-
75	A10	Output	MA8000 address output A10	-
76	A11	Output	MA8000 address output A11	-
77	A12	Output	MA8000 address output A12	-
78	A13	Output	MA8000 address output A13	-
79	A14	Output	MA8000 address output A14	-
80	A15	Output	MA8000 address output A15	-
81	XMPU	Input	MPU mode select	-
82	XCE	Output	External ROM chip select	-
83	XOE	Output	External ROM output enable	-
84	XWE	Output	External ROM write enable	-
85	D0	Input/Output	MA8000 data bus D0	-
86	D1	Input/Output	MA8000 data bus D1	-
87	D2	Input/Output	MA8000 data bus D2	-
88	D3	Input/Output	MA8000 data bus D3	-
89	D4	Input/Output	MA8000 data bus D4	-
90	D5	Input/Output	MA8000 data bus D5	-

91	D6	Input/Output	MA8000 data bus D6	-
92	D7	Input/Output	MA8000 data bus D7	-

The Input and I/O port are selectable by software for Nand-Flash & And-Flash function as follow :

	NAND-Flash			SD(MMC)-Card		AND-Flash	
	PAD	Name	I/O type	Name	I/O type	Name	I/O type
1	P00	IO0	I/O	DAT0	I/O	IO0	I/O
2	P01	IO1	I/O	DAT1(5)	I/O	IO1	I/O
3	P02	IO2	I/O	DAT2(5)	I/O	IO2	I/O
4	P03	IO3	I/O	CD/DAT3	I/O	IO3	I/O
5	P04	IO4	I/O	CMD	I/O	IO4	I/O
6	P05	IO5	I/O			IO5	I/O
7	P06	IO6	I/O			IO6	I/O
8	P07	IO7	I/O			IO7	I/O
9	P10	CLE	O			-CDE	O
10	P11	ALE	O			SC	O
11	P12						
12	P13						
13	P14	-RE	O			-OE	O
14	P15	-WE	O			-WE	O
15	P16	-CE	O			-CE	O
16	P17	-CE	O			-CE	O
17	P20			CLK	O		
18	P21	-CE	O			-CE	O
19	P22	-CE	O			-CE	O
20	P23	-CE	O			-CE	O
21	P24	-CE	O			-CE	O
22	P25	WP(2)			I	WP(2)	
23	P26						
24	P27						
25	P30	-CE	O			-CE	O
26	P31	-CE	O			-CE	O
27	P32			WP(2)			
28	P33						
29	K00						
30	K01						
31	K02			CD1(1)	I		
32	K03	R/-B(3)	I			R/-B(3)	I

Note 1. The Write Protect detect pin assign
S/W : The WP signal input pin can be selected by software.

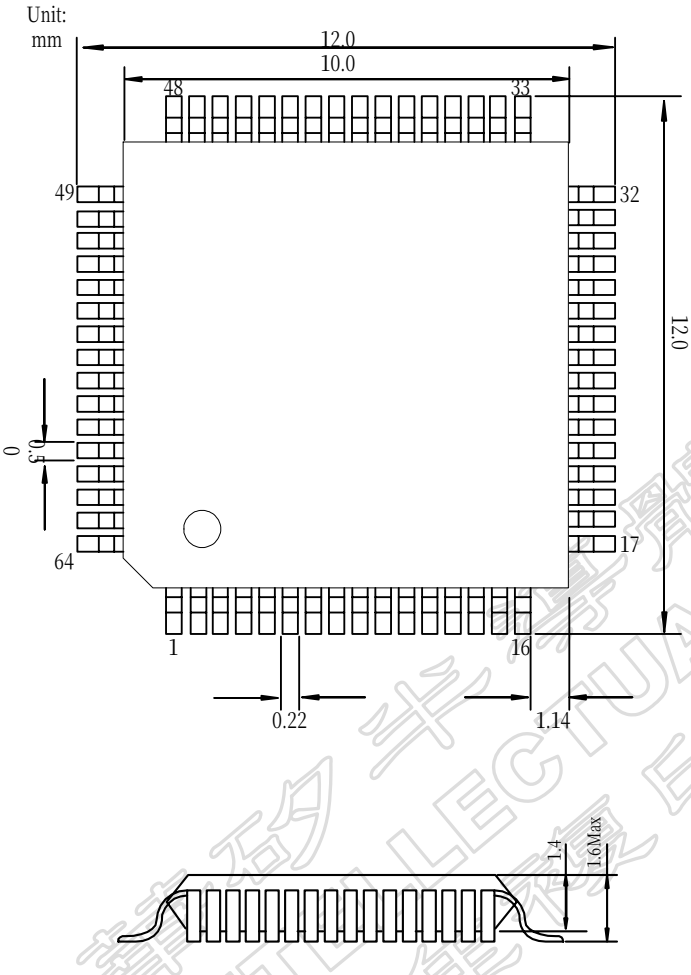
Note 2. The R/-B detect pin assign
There are two way to check the R/-B signal
S/W : The R/-B signal input pin can be selected by software to decide which Kport will be used.
H/W : The R/-B signal is checked by memory card controller and the R/-B signal input pin should follow the table suggested (K03).

Note 3. The Power Control pin assign
S/W : The Pwr_Ctrl output pin can be controlled by software.

Note 4. DAT1 and DAT2 are not used in MMC

2. PACKAGE AND DIMENSION

LQFP 64



3. CPU AND MEMOERY CONFIGURATION

In this section, we will explain the core CPU, operating mode and memory configuration.

3.1 CORE CPU

The WDC65C02C core offers complete hardware and software compatible with 6502 and many advantages of CMOS technology, including higher noise immunity, better reliability, and greatly reduced power requirements. The main features of the core CPU are:

1. Low power, static HCMOS implementation
2. 8-bit internal architecture with an 8-bit external data bus.
3. 21-bit address bus allows access to 4GByte of memory space
4. 16 addressing modes and 70 instructions
5. Hardware and software interrupts
6. Low power consumption (<1mA @1MHz)
7. Wait-for-interrupt (WAI) and Stop-the-Clock(STP) instructions further reduce power consumption, decrease interrupt latency and allows synchronization with external events

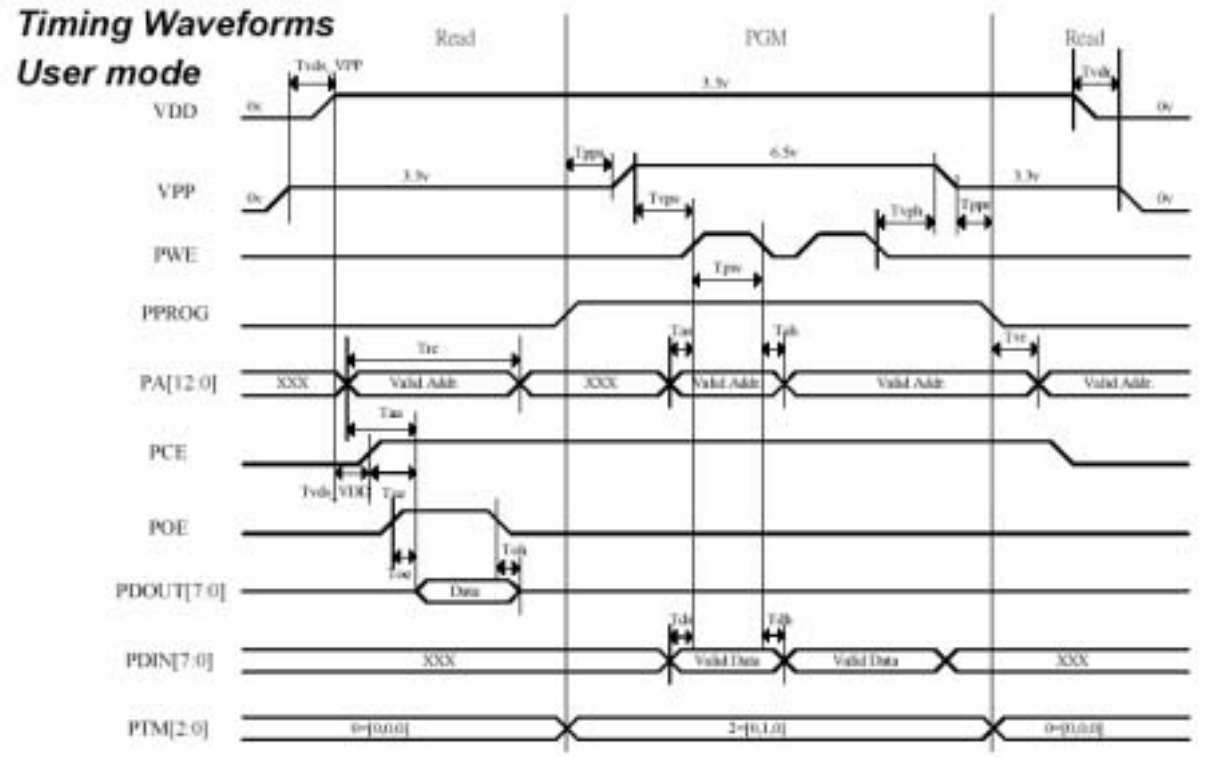
3.2 MEMORY MAP of EACH BLOCK

Address	Size	Description
0x0000 ~ 0x0FFF	4KB	Internal System RAM
0x1800 ~ 0x18FF	256B	I/O Control Registers
0x0000 ~ 0xFFFF	64KB	Internal OTP ROM

- ✧ The Internal system RAM, I/O Control Registers and Internal OTP are occupied each memory block.
- ✧ The 256 byte I/O memory is employed in the MA8201-H72 for interfacing with internal peripheral circuit. Peripheral circuit control bits and data registers are arranged in data memory space. Control and data-exchange are conducted via normal memory access.

3.2.1 OTP WRITE & READ

OTP read & write timing:



In OTP mode, we can use Pport & Kport to read & write OTP.

VPP = VD1
PWE = P07
PPROG = P06
PA[15:0] = P0[3:1], K0[5:1], P1[7:0]
PCE = P05
POE = P04
PDOUT[7:0] = P2[7:0]
PDIN[7:0] = P2[7:0]
PTM[2:0] = P3[3:1]

3.3 EXCEPTION PROCESSING VECTORS

Vector address	Exception-processing factor	Priority
0xFFFC	Reset	1
0xFFEA	PLL interrupt	
0xFFE8	UART interrupt	
0xFFE6	USB DMA interrupt	
0xFFE4	DMA	
0xFFE2	USB I/F interrupt	
0xFFE0	NAND FLASH interrupt	
0xFFDE	ADC interrupt	
0xFFDC	Secure Digital (SD) interrupt	
0xFFDA	SPI interrupt	
0xFFD8	Programmable timer 0 interrupt	
0xFFD6	Programmable timer 1 interrupt	
0xFFD4	Input port K0 interrupt	
0xFFD2	Clock Timer interrupt	
0xFFD0	CODEC interrupt	

Priority 1 has highest priority.

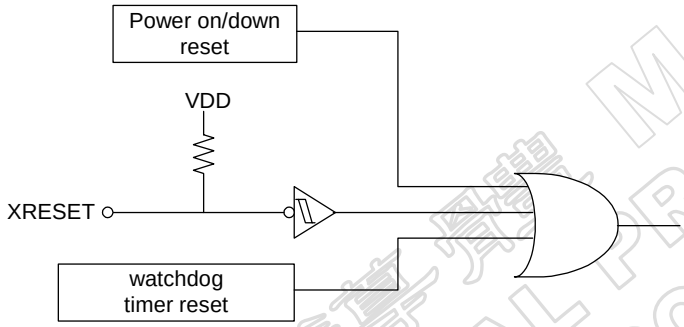
4. INITIAL RESET

Initial reset in the MA8201-H72 is required in order to initialize circuits. This section of the manual contains a description of initial reset factors and the initial settings for the internal registers, etc.

4.1 INITIAL RESET FACTORS

There are four initial reset factors for the MA8201-H72 as shown below.

1. XRESET terminal
2. Power on/down reset
3. Internal watchdog reset



The core CPU and peripheral circuit are initialized by means of initial reset factors. When the factor is canceled, the CPUs commence reset exception processing.
When this occurs, reset exception processing vectors, core CPU will execute from address 0xFFFC~0xFFFD.

4.1.1 XRESET TERMINAL

Initial reset can be done by asserting an external LOW level to the XRESET pin. Be sure to maintain the XRESET terminal at LOW level for the regulation time after the power on to assure the initial reset. In addition, be sure to use the XRESET terminal for the first initial reset after the power in turned on. The XRESET terminal is equipped with a pull-up resistor.

4.1.2 INTERNAL POWER ON/DOWN RESET

When the internal power on/down circuit detects a power supply voltage dropped below a certain criteria level, it will cause internal power on/down reset.

4.1.3 WATCHDOG TIMER RESET

When core CPU does not clear watchdog timer before the timer overflow, there will be a watchdog timer reset occurred when the timer is overflow.

4.2 USB SUSPEND I/O STATUS

When core CPU enter USB suspend mode, the I/O will enter the following status:

K00~K05 : Input without pull-up or pull-down resister
P00~P07 : Output "0" without pull-up or pull-down resister
P10~P15 : Output "0" without pull-up or pull-down resister
P16~P17 : Output "1" without pull-up or pull-down resister
P20~P26 : Output "0" without pull-up or pull-down resister
P27 : Output "1" without pull-up or pull-down resister
P30~P33 : Output "0" without pull-up or pull-down resister
P40~P47 : Output "0" without pull-up or pull-down resister

Some I/O ports special modify :
P24 : No pull-up resister selected (Remove the Resister by Hardware design)
P30 : Fix to Output port (Fix by Hardware design)
P30 : No pull-up resister selected (Remove the Resister by Hardware design)

5. PERIPHERAL CIRCUITS AND THEIR OPERATION

The peripheral circuits of the MA8201-H72 interface with the CPU by means of the memory mapped I/O method. For this reason, I/O memory of peripheral circuits can be addressed just like other memory access operations.

5.1 I/O MEMORY MAP

Watchdog and Port Function selection control registers

Address	Bit	Name	Function	1	0	SR	R/W
0x1800 SYS Control	D7	CLKCHG1	CPU(system) operating clock switch	00 : 32KHz 01 : 48MHz	10 : PLLCLK 11 : 48MHz	00	R/W
	D6	CLKCHG0					
	D5						
	D4	RCON	RC oscillator On/Off	On	Off	1	R/W
	D3	SCLK2	System clock for high speed clock select (EXCLK or PLLCLK)	000 : ExOsc 001 : ExOsc/2 010 : ExOsc/3 011 : ExOsc/4	100 : ExOsc/5 101 : ExOsc/6 110 : ExOsc/7 111 : ExOsc/8	001	R/W
	D2	SCLK1					
	D1	SCLK0					
	D0	EXCLKON	External Oscillator(48MHz) On/Off	On	Off	0	R/W
0x1801 SYS Control	D7	USBSUS	USB suspend request	Request	No request	0	R
	D6	PCSTBY	PC standby request	Request	No request	0	R
	D5	FWR2SUS	System ready to suspend	R Suspend W Ready	R Normal W none	0	R/W
	D4	SusThrd 2	The PC standby status detect threshold	T= 32* (SusThrd[2:0] +1) ms T=32ms – 256ms		1	R/W
	D3	SusThrd 1				1	R/W
	D2	SusThrd 0				1	R/W
	D1	WS1	Wait state	00 : 0 wait state 01 : 1 wait state 10 :2 wait state 11 : 3 wait state		00	R/W
	D0	WS0					
0x1802 SYS Control	D7						
	D6						
	D5	MPU_ST	CPU status	MPU	Normal	0	R
	D4	BUP	CLKIN oscillator speed up register	On	Off	1	R/W
	D3						
	D2						
	D1						
	D0	WDEN	Watchdog enable	enable	disable	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x1803 Watchdog Timer	D7	WDTRST	Reset watchdog timer	Reset	Normal	0	R/W
	D6	WDTP6	Watchdog time selection (1-128 sec.)	The watchdog time = 1-128 sec.		10H (17 sec)	R/W
	D5	WDTP5					
	D4	WDTP4					
	D3	WDTP3					
	D2	WDTP2					
	D1	WDTP1					
	D0	WDTP0					
0x1804 Port Function selection	D7	SPISEL1	P31-P33 I/O Port function selection	00 : Normal 01 : IIS	10 : SPI 11 : SPI	00	R/W
	D6	SPISEL0					
	D5	PXCE2	NAND Flash XCE pin select	000:P16 001:P17 010:P21 011:P22	100:P23 101:P24 110:P30 111:P31	000	R/W
	D4	PXCE1					
	D3	PXCE0					
	D2	PFSEL2	I/O Port function selection	100 : Port assign as NAND FLASH I/O 101 : Port assign as SD card I/O others : Normal I/O port		0	R/W
	D1	PFSEL1					
	D0	PFSEL0					
0x1805 Low power Control	D7	LPWDMA	DMA controller system clock stop	stop	Normal	0	R/W
	D6	LPWUSB	USB controller system clock stop	stop	Normal	0	R/W
	D5	LPWCTM	CTM controller system clock stop	stop	Normal	0	R/W
	D4	LPWPTM	PTM controller system clock stop	stop	Normal	0	R/W
	D3	LPWSPI	SPI controller system clock stop	stop	Normal	0	R/W
	D2	LPWSM	NAND FLASH controller system clock stop	stop	Normal	0	R/W
	D1	LPWSD	SD controller system clock stop	stop	Normal	0	R/W
	D0	LPWCODEC	CODEC decode system clock stop	stop	Normal	0	R/W
0x1806 Low power Control	D7	RSTDMA	DMA controller reset	reset	none	0	W
	D6	RSTUSB	USB controller reset	reset	none	0	W
	D5	RSTCTM	CTM controller reset	reset	none	0	W
	D4	RSTPTM	PTM controller reset	reset	none	0	W
	D3	RSTSPI	SPI controller reset	reset	none	0	W
	D2	RSTSM	NAND FLASH controller reset	reset	none	0	W
	D1	RSTSD	SD controller reset	reset	none	0	W
	D0	RSTCODEC	CODEC decode reset	reset	none	0	W

Address	Bit	Name	Function	1	0	SR	R/W
0x1807 Low power Control	D7						
	D6						
	D5						
	D4						
	D3	LPWADC	ADC controller system clock stop	stop	Normal	0	R/W
	D2	LPWUART	UART controller system clock stop	stop	Normal	0	R/W
	D1	LPW USBDMA	USB DMA controller system clock stop	stop	Normal	0	R/W
	D0						
0x1808 Low power Control	D7						
	D6						
	D5						
	D4						
	D3						
	D2	RSTUART	UART controller reset	reset	none	0	W
	D1	RST USBDMA	USB DMA controller reset	reset	none	0	W
	D0	RSTAD	AD controller reset	reset	none	0	W
0x1809 PLL	D7						
	D6						
	D5	IPLL	PLL interrupt factor flag	R: Yes / W: Reset	R: No / W: None	0	R/W
	D4	EIPLL	PLL interrupt mask register	Enable	Mask	0	R/W
	D3						
	D2	FpllCHG	Frequency change trigger register	Change	No change	0	W
	D1	PLLON	Turn on phase locked loop	Yes	No	0	R/W
	D0	DN8				0	W
0x180A PLL	D7	DN7	Phase locked loop (PLL) divide factor (DN8-DN0=5-512)	The PLL output : Fpll = divide factor * 32KHz		10H	R/W
	D6	DN6					
	D5	DN5					
	D4	DN4					
	D3	DN3					
	D2	DN2					
	D1	DN1					
	D0	DN0					

Address	Bit	Name	Function	1	0	SR	R/W
0x180B PLL	D7	DLY7	Phase locked loop (PLL) ready time (4ms*(DLY+1))	High	Low	0CH	R/W
	D6	DLY6		High	Low		
	D5	DLY5		High	Low		
	D4	DLY4		High	Low		
	D3	DLY3		High	Low		
	D2	DLY2		High	Low		
	D1	DLY1		High	Low		
	D0	DLY0		High	Low		

Input port control registers

Address	Bit	Name	Function	1	0	SR	R/W
0x1810 Input Port	D7						
	D6						
	D5	KIT05	Input port K05 interrupt trigger mode	Falling	Rising	1	R/W
	D4	KIT04	Input port K04 interrupt trigger mode	Falling	Rising	1	R/W
	D3	KIT03	Input port K03 interrupt trigger mode	Falling	Rising	1	R/W
	D2	KIT02	Input port K02 interrupt trigger mode	Falling	Rising	1	R/W
	D1	KIT01	Input port K01 interrupt trigger mode	Falling	Rising	1	R/W
	D0	KIT00	Input port K00 interrupt trigger mode	Falling	Rising	1	R/W
0x1811 Input Port	D7						
	D6						
	D5	K05R	Input port K05 pull-up resister select	On	Off	1	R/W
	D4	K04R	Input port K04 pull-up resister select	On	Off	1	R/W
	D3	K03R	Input port K03 pull-up resister select	On	Off	1	R/W
	D2	K02R	Input port K02 pull-up resister select	On	Off	1	R/W
	D1	K01R	Input port K01 pull-up resister select	On	Off	1	R/W
	D0	K00R	Input port K00 pull-up resister select	On	Off	1	R/W
0x1812 Input Port	D7						
	D6						
	D5	K05N	Input port K05 noise reject select	With noise rej.	No noise rej.	0	R/W
	D4	K04N	Input port K04 noise reject select	With noise rej.	No noise rej.	0	R/W
	D3	K03N	Input port K03 noise reject select	With noise rej.	No noise rej.	0	R/W
	D2	K02N	Input port K02 noise reject select	With noise rej.	No noise rej.	0	R/W
	D1	K01N	Input port K01 noise reject select	With noise rej.	No noise rej.	0	R/W
	D0	K00N	Input port K00 noise reject select	With noise rej.	No noise rej.	0	R/W
0x1813 Input Port	D7						
	D6						
	D5	K05	Input port K05 data	High	Low		R
	D4	K04	Input port K04 data	High	Low		R
	D3	K03	Input port K03 data	High	Low		R
	D2	K02	Input port K02 data	High	Low		R
	D1	K01	Input port K01 data	High	Low		R
	D0	K00	Input port K00 data	High	Low		R

Address	Bit	Name	Function	1		0		SR	R/W
0x1814 Input Port	D7								
	D6								
	D5								
	D4								
	D3								
	D2								
	D1								
	D0	IK0	Input port K05-K00 interrupt factor flag	R W	Yes Reset	R W	No None	0	R/W
0x1815 Input Port	D7								
	D6								
	D5	EIK05	Input port K05 interrupt mask register	Enable		Mask		0	R/W
	D4	EIK04	Input port K04 interrupt mask register	Enable		Mask		0	R/W
	D3	EIK03	Input port K03 interrupt mask register	Enable		Mask		0	R/W
	D2	EIK02	Input port K02 interrupt mask register	Enable		Mask		0	R/W
	D1	EIK01	Input port K01 interrupt mask register	Enable		Mask		0	R/W
	D0	EIK00	Input port K00 interrupt mask register	Enable		Mask		0	R/W

I/O port control registers (P07-P00)

Address	Bit	Name	Function	1	0	SR	R/W
0x1820 I/O Port	D7	P07D	Input/output port P07 direction select	Output	Input	0	R/W
	D6	P06D	Input/output port P06 direction select	Output	Input	0	R/W
	D5	P05D	Input/output port P05 direction select	Output	Input	0	R/W
	D4	P04D	Input/output port P04 direction select	Output	Input	0	R/W
	D3	P03D	Input/output port P03 direction select	Output	Input	0	R/W
	D2	P02D	Input/output port P02 direction select	Output	Input	0	R/W
	D1	P01D	Input/output port P01 direction select	Output	Input	0	R/W
	D0	P00D	Input/output port P00 direction select	Output	Input	0	R/W
0x1821 I/O Port	D7	P07R	P07 pull-up resister select	On	Off	1	R/W
	D6	P06R	P06 pull-up resister select	On	Off	1	R/W
	D5	P05R	P05 pull-up resister select	On	Off	1	R/W
	D4	P04R	P04 pull-up resister select	On	Off	1	R/W
	D3	P03R	P03 pull-up resister select	On	Off	1	R/W
	D2	P02R	P02 pull-up resister select	On	Off	1	R/W
	D1	P01R	P01 pull-up resister select	On	Off	1	R/W
	D0	P00R	P00 pull-up resister select	On	Off	1	R/W
0x1822 I/O Port	D7	P07	Input/output port P07 data	High	Low	1	R/W
	D6	P06	Input/output port P06 data	High	Low	1	R/W
	D5	P05	Input/output port P05 data	High	Low	1	R/W
	D4	P04	Input/output port P04 data	High	Low	1	R/W
	D3	P03	Input/output port P03 data	High	Low	1	R/W
	D2	P02	Input/output port P02 data	High	Low	1	R/W
	D1	P01	Input/output port P01 data	High	Low	1	R/W
	D0	P00	Input/output port P00 data	High	Low	1	R/W

I/O port control registers (P17-P10)

Address	Bit	Name	Function	1	0	SR	R/W
0x1823 I/O Port	D7	P17D	Input/output port P17 direction select	Output	Input	0	R/W
	D6	P16D	Input/output port P16 direction select	Output	Input	0	R/W
	D5	P15D	Input/output port P15 direction select	Output	Input	0	R/W
	D4	P14D	Input/output port P14direction select	Output	Input	0	R/W
	D3	P13D	Input/output port P13 direction select	Output	Input	0	R/W
	D2	P12D	Input/output port P12 direction select	Output	Input	0	R/W
	D1	P11D	Input/output port P11 direction select	Output	Input	0	R/W
	D0	P10D	Input/output port P10 direction select	Output	Input	0	R/W
0x1824 I/O Port	D7	P17R	P17 pull-up resister select	On	Off	1	R/W
	D6	P16R	P16 pull-up resister select	On	Off	1	R/W
	D5	P15R	P15 pull-up resister select	On	Off	1	R/W
	D4	P14R	P14 pull-up resister select	On	Off	1	R/W
	D3	P13R	P13 pull-up resister select	On	Off	1	R/W
	D2	P12R	P12 pull-up resister select	On	Off	1	R/W
	D1	P11R	P11 pull-up resister select	On	Off	1	R/W
	D0	P10R	P10 pull-up resister select	On	Off	1	R/W
0x1825 I/O Port	D7	P17	Input/output port P17 data	High	Low	1	R/W
	D6	P16	Input/output port P16 data	High	Low	1	R/W
	D5	P15	Input/output port P15 data	High	Low	1	R/W
	D4	P14	Input/output port P14 data	High	Low	1	R/W
	D3	P13	Input/output port P13 data	High	Low	1	R/W
	D2	P12	Input/output port P12 data	High	Low	1	R/W
	D1	P11	Input/output port P11 data	High	Low	1	R/W
	D0	P10	Input/output port P10 data	High	Low	1	R/W

I/O port control registers (P27-P20)

Address	Bit	Name	Function	1	0	SR	R/W
0x1826 I/O Port	D7	P27D	Input/output port P27 direction select	Output	Input	0	R/W
	D6	P26D	Input/output port P26 direction select	Output	Input	0	R/W
	D5	P25D	Input/output port P25 direction select	Output	Input	0	R/W
	D4	P24D	Input/output port P24 direction select	Output	Input	0	R/W
	D3	P23D	Input/output port P23 direction select	Output	Input	0	R/W
	D2	P22D	Input/output port P22 direction select	Output	Input	0	R/W
	D1	P21D	Input/output port P21 direction select	Output	Input	0	R/W
	D0	P20D	Input/output port P20 direction select	Output	Input	0	R/W
0x1827 I/O Port	D7	P27R	P27 pull-up resister select	On	Off	1	R/W
	D6	P26R	P26 pull-up resister select	On	Off	1	R/W
	D5	P25R	P25 pull-up resister select	On	Off	1	R/W
	D4	P24R	P24 pull-up resister select	On	Off	1	R/W
	D3	P23R	P23 pull-up resister select	On	Off	1	R/W
	D2	P22R	P22 pull-up resister select	On	Off	1	R/W
	D1	P21R	P21 pull-up resister select	On	Off	1	R/W
	D0	P20R	P20 pull-up resister select	On	Off	1	R/W
0x1828 I/O Port	D7	P27	Input/output port P27 data	High	Low	1	R/W
	D6	P26	Input/output port P26 data	High	Low	1	R/W
	D5	P25	Input/output port P25 data	High	Low	1	R/W
	D4	P24	Input/output port P24 data	High	Low	1	R/W
	D3	P23	Input/output port P23 data	High	Low	1	R/W
	D2	P22	Input/output port P22 data	High	Low	1	R/W
	D1	P21	Input/output port P21 data	High	Low	1	R/W
	D0	P20	Input/output port P20 data	High	Low	1	R/W

I/O port control registers (P33-P30)

Address	Bit	Name	Function	1	0	SR	R/W
0x1829 I/O Port	D7						
	D6						
	D5						
	D4						
	D3	P33D	Input/output port P33 direction select	Output	Input	0	R/W
	D2	P32D	Input/output port P32 direction select	Output	Input	0	R/W
	D1	P31D	Input/output port P31 direction select	Output	Input	0	R/W
	D0	P30D	Input/output port P30 direction select	Output	Input	0	R/W
0x182A I/O Port	D7						
	D6						
	D5						
	D4						
	D3	P33R	P33 pull-up resister select	On	Off	1	R/W
	D2	P32R	P32 pull-up resister select	On	Off	1	R/W
	D1	P31R	P31 pull-up resister select	On	Off	1	R/W
	D0	P30R	P30 pull-up resister select	On	Off	1	R/W
0x182B I/O Port	D7						
	D6						
	D5						
	D4						
	D3	P33	Input/output port P33 data	High	Low	1	R/W
	D2	P32	Input/output port P32 data	High	Low	1	R/W
	D1	P31	Input/output port P31 data	High	Low	1	R/W
	D0	P30	Input/output port P30 data	High	Low	1	R/W

I/O port control registers (P47-P40)

Address	Bit	Name	Function	1	0	SR	R/W
0x182C I/O Port	D7	P47D	Input/output port P47 direction select	Output	Input	0	R/W
	D6	P46D	Input/output port P46 direction select	Output	Input	0	R/W
	D5	P45D	Input/output port P45 direction select	Output	Input	0	R/W
	D4	P44D	Input/output port P44direction select	Output	Input	0	R/W
	D3	P43D	Input/output port P43 direction select	Output	Input	0	R/W
	D2	P42D	Input/output port P42 direction select	Output	Input	0	R/W
	D1	P41D	Input/output port P41 direction select	Output	Input	0	R/W
	D0	P40D	Input/output port P40 direction select	Output	Input	0	R/W
0x182D I/O Port	D7	P47R	P47 pull-up resister select	On	Off	1	R/W
	D6	P46R	P46 pull-up resister select	On	Off	1	R/W
	D5	P45R	P45 pull-up resister select	On	Off	1	R/W
	D4	P44R	P44 pull-up resister select	On	Off	1	R/W
	D3	P43R	P43 pull-up resister select	On	Off	1	R/W
	D2	P42R	P42 pull-up resister select	On	Off	1	R/W
	D1	P41R	P41 pull-up resister select	On	Off	1	R/W
	D0	P40R	P40 pull-up resister select	On	Off	1	R/W
0x182E I/O Port	D7	P47	Input/output port P47 data	High	Low	1	R/W
	D6	P46	Input/output port P46 data	High	Low	1	R/W
	D5	P45	Input/output port P45 data	High	Low	1	R/W
	D4	P44	Input/output port P44 data	High	Low	1	R/W
	D3	P43	Input/output port P43 data	High	Low	1	R/W
	D2	P42	Input/output port P42 data	High	Low	1	R/W
	D1	P41	Input/output port P41 data	High	Low	1	R/W
	D0	P40	Input/output port P40 data	High	Low	1	R/W

Clock Timer control registers

Address	Bit	Name	Function	1	0	SR	R/W
0x1830 Clock Timer	D7						
	D6						
	D5						
	D4						
	D3						
	D2						
	D1	CTRST	Clock timer reset	Reset	No operation	-	W
	D0	CTRUN	Clock timer Run/Stop control	Run	Stop	0	R/W
0x1831 Clock Timer	D7	CT1D	Clock timer data 1 Hz	High	Low	0	R
	D6	CT2D	Clock timer data 2 Hz				
	D5	CT4D	Clock timer data 4 Hz				
	D4	CT8D	Clock timer data 8 Hz				
	D3	CT16D	Clock timer data 16 Hz				
	D2	CT32D	Clock timer data 32 Hz				
	D1	CT64D	Clock timer data 64 Hz				
	D0	CT128D	Clock timer data 128 Hz				
0x1832 Clock Timer	D7						
	D6	ICT64	Clock timer 64 Hz interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D5	ICT32	Clock timer 32 Hz interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D4	ICT16	Clock timer 16 Hz interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D3	ICT8	Clock timer 8 Hz interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D2	ICT4	Clock timer 4 Hz interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D1	ICT2	Clock timer 2 Hz interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D0	ICT1	Clock timer 1 Hz interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
0x1833 Clock Timer	D7						
	D6	ECT64	Clock timer 64 Hz interrupt mask register	Enable	Mask	0	R/W
	D5	ECT32	Clock timer 32 Hz interrupt mask register	Enable	Mask	0	R/W
	D4	ECT16	Clock timer 16 Hz interrupt mask register	Enable	Mask	0	R/W
	D3	ECT8	Clock timer 8 Hz interrupt mask register	Enable	Mask	0	R/W
	D2	ECT4	Clock timer 4 Hz interrupt mask register	Enable	Mask	0	R/W
	D1	ECT2	Clock timer 2 Hz interrupt mask register	Enable	Mask	0	R/W
	D0	ECT1	Clock timer 1 Hz interrupt mask register	Enable	Mask	0	R/W

RC Oscillator Timer registers

Address	Bit	Name	Function	1	0	SR	R/W
0x184E RC Osc. Timer	D7	RCD15	RC Timer data 15	High	Low	0	R
	D6	RCD14	RC Timer data 14	High	Low	0	R
	D5	RCD13	RC Timer data 13	High	Low	0	R
	D4	RCD12	RC Timer data 12	High	Low	0	R
	D3	RCD11	RC Timer data 11	High	Low	0	R
	D2	RCD10	RC Timer data 10	High	Low	0	R
	D1	RCD9	RC Timer data 9	High	Low	0	R
	D0	RCD8	RC Timer data 8	High	Low	0	R
0x184F RC Osc. Timer	D7	RCD7	RC Timer data 7	High	Low	0	R
	D6	RCD6	RC Timer data 6	High	Low	0	R
	D5	RCD5	RC Timer data 5	High	Low	0	R
	D4	RCD4	RC Timer data 4	High	Low	0	R
	D3	RCD3	RC Timer data 3	High	Low	0	R
	D2	RCD2	RC Timer data 2	High	Low	0	R
	D1	RCD1	RC Timer data 1	High	Low	0	R
	D0	RCD0	RC Timer data 0	High	Low	0	R

Programmable Timer 0 & 1 control registers

Address	Bit	Name	Function	1		0		SR	R/W
0x1840 Prog. Timer0	D7								
	D6								
	D5								
	D4								
	D3								
	D2								
	D1	IP0	Timer0 interrupt factor flag	R W	Yes Reset	R W	No None	0	R/W
	D0	EIP0	Timer0 interrupt mask register	Enable		Mask		0	R/W
0x1841 Prog. Timer0	D7								
	D6	P0SET	Timer0 preset	Preset		None		0	W
	D5	P0RUN	Timer0 run/stop control	Run		Stop		0	R/W
	D4								
	D3	P0CONT	Timer0 continuous/one shot select	Continuous		One shot		0	R/W
	D2	P0CKSEL	Programmable timer0 clock source	Fosc3		32KHz		0	R/W
	D1	P0SC1	Programmable timer0 pre-scale clock source selection	00 : clock/1 01 : clock/4		10 : clock/16 11: clock/64		00	R/W
	D0	P0SC0							
0x1842 Prog. Timer0	D7	P0RLD7	Timer0 reload data D7	High		Low		0	R/W
	D6	P0RLD6	Timer0 reload data D6	High		Low		0	R/W
	D5	P0RLD5	Timer0 reload data D5	High		Low		0	R/W
	D4	P0RLD4	Timer0 reload data D4	High		Low		0	R/W
	D3	P0RLD3	Timer0 reload data D3	High		Low		0	R/W
	D2	P0RLD2	Timer0 reload data D2	High		Low		0	R/W
	D1	P0RLD1	Timer0 reload data D1	High		Low		0	R/W
	D0	P0RLD0	Timer0 reload data D0 (LSB)	High		Low		0	R/W
0x1843 Prog. Timer0	D7	P0RLD15	Timer0 reload data D15 (MSB)	High		Low		0	R/W
	D6	P0RLD14	Timer0 reload data D14	High		Low		0	R/W
	D5	P0RLD13	Timer0 reload data D13	High		Low		0	R/W
	D4	P0RLD12	Timer0 reload data D12	High		Low		0	R/W
	D3	P0RLD11	Timer0 reload data D11	High		Low		0	R/W
	D2	P0RLD10	Timer0 reload data D10	High		Low		0	R/W
	D1	P0RLD9	Timer0 reload data D9	High		Low		0	R/W
	D0	P0RLD8	Timer0 reload data D8	High		Low		0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x1844 Prog. Timer0	D7	P0TD7	Timer0 counter data D7	High	Low		R
	D6	P0TD6	Timer0 counter data D6	High	Low		R
	D5	P0TD5	Timer0 counter data D5	High	Low		R
	D4	P0TD4	Timer0 counter data D4	High	Low		R
	D3	P0TD3	Timer0 counter data D3	High	Low		R
	D2	P0TD2	Timer0 counter data D2	High	Low		R
	D1	P0TD1	Timer0 counter data D1	High	Low		R
	D0	P0TD0	Timer0 counter data D0 (LSB)	High	Low		R
0x1845 Prog. Timer0	D7	P0TD15	Timer0 counter data D15 (MSB)	High	Low		R
	D6	P0TD14	Timer0 counter data D14	High	Low		R
	D5	P0TD13	Timer0 counter data D13	High	Low		R
	D4	P0TD12	Timer0 counter data D12	High	Low		R
	D3	P0TD11	Timer0 counter data D11	High	Low		R
	D2	P0TD10	Timer0 counter data D10	High	Low		R
	D1	P0TD9	Timer0 counter data D9	High	Low		R
	D0	P0TD8	Timer0 counter data D8	High	Low		R
0x1848 Prog. Timer1	D7						
	D6						
	D5						
	D4						
	D3						
	D2						
	D1	IP1	Timer1 interrupt factor flag	R Yes W Reset	R No W None	0	R/W
	D0	EIP1	Timer1 interrupt mask register	Enable	Mask	0	R/W
0x1849 Prog. Timer1	D7						
	D6	P1SET	Timer1 preset	Preset	None	0	W
	D5	P1RUN	Timer1 run/stop control	Run	Stop	0	R/W
	D4						
	D3	P1CONT	Timer1 continuous/one shot select	Continuous	One shot	0	R/W
	D2	P1CKSEL	Programmable timer1 clock source	Fosc3	32KHz	0	R/W
	D1	P1SC1	Programmable timer1 pre-scale clock source selection	00 : clock/1 01 : clock/4	10 : clock/16 11: clock/64	00	R/W
	D0	P1SC0					

Address	Bit	Name	Function	1	0	SR	R/W
0x184A Prog. Timer1	D7	P1RLD7	Timer1 reload data D7	High	Low	0	R/W
	D6	P1RLD6	Timer1 reload data D6	High	Low	0	R/W
	D5	P1RLD5	Timer1 reload data D5	High	Low	0	R/W
	D4	P1RLD4	Timer1 reload data D4	High	Low	0	R/W
	D3	P1RLD3	Timer1 reload data D3	High	Low	0	R/W
	D2	P1RLD2	Timer1 reload data D2	High	Low	0	R/W
	D1	P1RLD1	Timer1 reload data D1	High	Low	0	R/W
	D0	P1RLD0	Timer1 reload data D0 (LSB)	High	Low	0	R/W
0x184B Prog. Timer1	D7	P1RLD15	Timer1 reload data D15 (MSB)	High	Low	0	R/W
	D6	P1RLD14	Timer1 reload data D14	High	Low	0	R/W
	D5	P1RLD13	Timer1 reload data D13	High	Low	0	R/W
	D4	P1RLD12	Timer1 reload data D12	High	Low	0	R/W
	D3	P1RLD11	Timer1 reload data D11	High	Low	0	R/W
	D2	P1RLD10	Timer1 reload data D10	High	Low	0	R/W
	D1	P1RLD9	Timer1 reload data D9	High	Low	0	R/W
	D0	P1RLD8	Timer1 reload data D8	High	Low	0	R/W
0x184C Prog. Timer1	D7	P1TD7	Timer1 counter data D7	High	Low	0	R
	D6	P1TD6	Timer1 counter data D6	High	Low	0	R
	D5	P1TD5	Timer1 counter data D5	High	Low	0	R
	D4	P1TD4	Timer1 counter data D4	High	Low	0	R
	D3	P1TD3	Timer1 counter data D3	High	Low	0	R
	D2	P1TD2	Timer1 counter data D2	High	Low	0	R
	D1	P1TD1	Timer1 counter data D1	High	Low	0	R
	D0	P1TD0	Timer1 counter data D0 (LSB)	High	Low	0	R
0x184D Prog. Timer1	D7	P1TD15	Timer1 counter data D15 (MSB)	High	Low	0	R
	D6	P1TD14	Timer1 counter data D14	High	Low	0	R
	D5	P1TD13	Timer1 counter data D13	High	Low	0	R
	D4	P1TD12	Timer1 counter data D12	High	Low	0	R
	D3	P1TD11	Timer1 counter data D11	High	Low	0	R
	D2	P1TD10	Timer1 counter data D10	High	Low	0	R
	D1	P1TD9	Timer1 counter data D9	High	Low	0	R
	D0	P1TD8	Timer1 counter data D8	High	Low	0	R

NAND Flash Memory control registers

Map for NAND Flash

Address	Bit	Name	Function	1	0	SR	R/W
0x1850 NAND FLASH	D7	SMPA7	NAND FLASH page address PA7	High	Low	0	R/W
	D6	SMPA6	NAND FLASH page address PA6	High	Low	0	R/W
	D5	SMPA5	NAND FLASH page address PA5	High	Low	0	R/W
	D4	SMPA4	NAND FLASH page address PA4	High	Low	0	R/W
	D3	SMPA3	NAND FLASH page address PA3	High	Low	0	R/W
	D2	SMPA2	NAND FLASH page address PA2	High	Low	0	R/W
	D1	SMPA1	NAND FLASH page address PA1	High	Low	0	R/W
	D0	SMPA0	NAND FLASH page address PA0	High	Low	0	R/W
0x1851 NAND FLASH	D7	SMPA15	NAND FLASH page address PA15	High	Low	0	R/W
	D6	SMPA14	NAND FLASH page address PA14	High	Low	0	R/W
	D5	SMPA13	NAND FLASH page address PA13	High	Low	0	R/W
	D4	SMPA12	NAND FLASH page address PA12	High	Low	0	R/W
	D3	SMPA11	NAND FLASH page address PA11	High	Low	0	R/W
	D2	SMPA10	NAND FLASH page address PA10	High	Low	0	R/W
	D1	SMPA9	NAND FLASH page address PA9	High	Low	0	R/W
	D0	SMPA8	NAND FLASH page address PA8	High	Low	0	R/W
0x1852 NAND FLASH	D7	SMPA23	NAND FLASH page address PA23	High	Low	0	R/W
	D6	SMPA22	NAND FLASH page address PA22	High	Low	0	R/W
	D5	SMPA21	NAND FLASH page address PA21	High	Low	0	R/W
	D4	SMPA20	NAND FLASH page address PA20	High	Low	0	R/W
	D3	SMPA19	NAND FLASH page address PA19	High	Low	0	R/W
	D2	SMPA18	NAND FLASH page address PA18	High	Low	0	R/W
	D1	SMPA17	NAND FLASH page address PA17	High	Low	0	R/W
	D0	SMPA16	NAND FLASH page address PA16	High	Low	0	R/W
0x1853 NAND FLASH	D7	SMCA7	NAND FLASH column address CA7	High	Low	0	R/W
	D6	SMCA6	NAND FLASH column address CA6	High	Low	0	R/W
	D5	SMCA5	NAND FLASH column address CA5	High	Low	0	R/W
	D4	SMCA4	NAND FLASH column address CA4	High	Low	0	R/W
	D3	SMCA3	NAND FLASH column address CA3	High	Low	0	R/W
	D2	SMCA2	NAND FLASH column address CA2	High	Low	0	R/W
	D1	SMCA1	NAND FLASH column address CA1	High	Low	0	R/W
	D0	SMCA0	NAND FLASH column address CA0	High	Low	0	R/W

Map for NAND FLASH

Address	Bit	Name	Function	1	0	SR	R/W
0x1854 NAND FLASH	D7	SMD7	Read/Write data buffer	High	Low	0	R/W
	D6	SMD6		High	Low	0	R/W
	D5	SMD5		High	Low	0	R/W
	D4	SMD4		High	Low	0	R/W
	D3	SMD3		High	Low	0	R/W
	D2	SMD2		High	Low	0	R/W
	D1	SMD1		High	Low	0	R/W
	D0	SMD0		High	Low	0	R/W
0x1855 NAND FLASH	D7						
	D6						
	D5	ISMXCD	Card detect on interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D4	ISMXBY	Busy end interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D3	ISMEND	Block finish interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D2	EISMXCD	Card detect interrupt mask register	Enable	Mask	0	R/W
	D1	EISMXBY	Ready/busy interrupt mask register	Enable	Mask	0	R/W
	D0	EISMEND	Block finish interrupt mask register	Enable	Mask	0	R/W
0x1856 NAND & AND FLASH	D7	ENSM	Chip Select on/off	On	Off	0	R/W
	D6						
	D5	SMRUN	Interface run	Run	None		W
	D4						
	D3	FOEL	Force AND Flash OE Low	Force Low	Normal	0	R/W
	D2	FCH	Force AND Flash CDE High	Force High	Normal	0	R/W
	D1	SMOP1	Operating mode select	0 : command 1 : address write	2 : data write 3 : data read	00	R/W
	D0	SMOP0					
0x1857 NAND & AND FLASH	D7	SMAM	Access Method	By hardware	By CPU	0	R/W
	D6	SMCLK2	Data rate select	000 : clock/2 001 : clock/4 010 : clock/8 011 : clock/16	100 : clock/32 101 : clock/64 110 : clock/128 111 : clock/256	000	R/W
	D5	SMCLK1					
	D4	SMCLK0					
	D3	SMBKL	Data Transfer Block Length	Block Length = 2^SMBKL BKL=0 ~ 12		0	R/W
	D2						
	D1						
	D0						

Address	Bit	Name	Function	1	0	SR	R/W
0x1858 NAND & AND FLASH	D7						
	D6						
	D5	ODD	Odd or even	Odd	Even	0	R/W
	D4						
	D3						
	D2						
	D1	MODE	Read or write	write	read	0	R/W
	D0	STC	ECC start	start	stop	0	R/W
0x1859 NAND & AND FLASH	D7	LP7A	ECC function	High	Low	0	R
	D6	LP6A	ECC function	High	Low	0	R
	D5	LP5A	ECC function	High	Low	0	R
	D4	LP4A	ECC function	High	Low	0	R
	D3	LP3A	ECC function	High	Low	0	R
	D2	LP2A	ECC function	High	Low	0	R
	D1	LP1A	ECC function	High	Low	0	R
	D0	LP0A	ECC function	High	Low	0	R
0x185A NAND & AND FLASH	D7	LP15A	ECC function	High	Low	0	R
	D6	LP14A	ECC function	High	Low	0	R
	D5	LP13A	ECC function	High	Low	0	R
	D4	LP12A	ECC function	High	Low	0	R
	D3	LP11A	ECC function	High	Low	0	R
	D2	LP10A	ECC function	High	Low	0	R
	D1	LP9A	ECC function	High	Low	0	R
	D0	LP8A	ECC function	High	Low	0	R
0x185B NAND & AND FLASH	D7	CP5A	ECC function	High	Low	0	R
	D6	CP4A	ECC function	High	Low	0	R
	D5	CP3A	ECC function	High	Low	0	R
	D4	CP2A	ECC function	High	Low	0	R
	D3	CP1A	ECC function	High	Low	0	R
	D2	CP0A	ECC function	High	Low	0	R
	D1	ECCT1A	When odd is true, ECCT1A=1	Odd	Even	0	R
	D0	ECCT0A	When odd is true, ECCT0A=1	Odd	Even	0	R

Address	Bit	Name	Function	1	0	SR	R/W
0x185C NAND & AND FLASH	D7	LP7B	ECC function	High	Low	0	R
	D6	LP6B	ECC function	High	Low	0	R
	D5	LP5B	ECC function	High	Low	0	R
	D4	LP4B	ECC function	High	Low	0	R
	D3	LP3B	ECC function	High	Low	0	R
	D2	LP2B	ECC function	High	Low	0	R
	D1	LP1B	ECC function	High	Low	0	R
	D0	LP0B	ECC function	High	Low	0	R
0x185D NAND & AND FLASH	D7	LP15B	ECC function	High	Low	0	R
	D6	LP14B	ECC function	High	Low	0	R
	D5	LP13B	ECC function	High	Low	0	R
	D4	LP12B	ECC function	High	Low	0	R
	D3	LP11B	ECC function	High	Low	0	R
	D2	LP10B	ECC function	High	Low	0	R
	D1	LP9B	ECC function	High	Low	0	R
	D0	LP8B	ECC function	High	Low	0	R
0x185E NAND & AND FLASH	D7	CP5B	ECC function	High	Low	0	R
	D6	CP4B	ECC function	High	Low	0	R
	D5	CP3B	ECC function	High	Low	0	R
	D4	CP2B	ECC function	High	Low	0	R
	D3	CP1B	ECC function	High	Low	0	R
	D2	CP0B	ECC function	High	Low	0	R
	D1	ECCT1B	When odd is true, ECCT1B=1	Odd	Even	0	R
	D0	ECCT0B	When odd is true, ECCT0B=1	Odd	Even	0	R
0x185F NAND FLASH	D7	SMWA2	Address write mode (000: SMPA20-0 & SMCA7-0; 010: SMPA15-0 & SMCA7-0; 100: SMPA20-SMPA0; 110: SMPA15-SMPA0; 001: SMPA20-0 & SMCA11-0; 011: SMPA20-0 & SMCA15-0); 100&110 only use at Block Erase command			00	R/W
	D6	SMWA1					
	D5	SMWA0					
	D4	SMCA12	NAND FLASH column address CA12	High	Low	0	R/W
	D3	SMCA11	NAND FLASH column address CA11	High	Low	0	R/W
	D2	SMCA10	NAND FLASH column address CA10	High	Low	0	R/W
	D1	SMCA9	NAND FLASH column address CA9	High	Low	0	R/W
	D0	SMCA8	NAND FLASH column address CA8	High	Low	0	R/W

Map for AND Flash

Address	Bit	Name	Function	1	0	SR	R/W
0x1850 AND FLASH	D7	ANDSA7	AND FLASH sector address SA7	High	Low	0	R/W
	D6	ANDSA6	AND FLASH sector address SA6	High	Low	0	R/W
	D5	ANDSA5	AND FLASH sector address SA5	High	Low	0	R/W
	D4	ANDSA4	AND FLASH sector address SA4	High	Low	0	R/W
	D3	ANDSA3	AND FLASH sector address SA3	High	Low	0	R/W
	D2	ANDSA2	AND FLASH sector address SA2	High	Low	0	R/W
	D1	ANDSA1	AND FLASH sector address SA1	High	Low	0	R/W
	D0	ANDSA0	AND FLASH sector address SA0	High	Low	0	R/W
0x1851 AND FLASH	D7	ANDSA15	AND FLASH sector address SA15	High	Low	0	R/W
	D6	ANDSA14	AND FLASH sector address SA14	High	Low	0	R/W
	D5	ANDSA13	AND FLASH sector address SA13	High	Low	0	R/W
	D4	ANDSA12	AND FLASH sector address SA12	High	Low	0	R/W
	D3	ANDSA11	AND FLASH sector address SA11	High	Low	0	R/W
	D2	ANDSA10	AND FLASH sector address SA10	High	Low	0	R/W
	D1	ANDSA9	AND FLASH sector address SA9	High	Low	0	R/W
	D0	ANDSA8	AND FLASH sector address SA8	High	Low	0	R/W
0x1853 AND FLASH	D7	ANDCA7	AND FLASH column address CA7	High	Low	0	R/W
	D6	ANDCA6	AND FLASH column address CA6	High	Low	0	R/W
	D5	ANDCA5	AND FLASH column address CA5	High	Low	0	R/W
	D4	ANDCA4	AND FLASH column address CA4	High	Low	0	R/W
	D3	ANDCA3	AND FLASH column address CA3	High	Low	0	R/W
	D2	ANDCA2	AND FLASH column address CA2	High	Low	0	R/W
	D1	ANDCA1	AND FLASH column address CA1	High	Low	0	R/W
	D0	ANDCA0	AND FLASH column address CA0	High	Low	0	R/W
0x185F AND FLASH	D7	ANDWA2	Address write mode: (010: SMSA15-0, 101: SMCA12-0, 111: SMSA15-0 & SMCA11-0)			0	R/W
	D6	ANDWA1				0	R/W
	D5	ANDWA0				0	R/W
	D4	ANDCA12	AND FLASH column address CA12	High	Low	0	R/W
	D3	ANDCA11	AND FLASH column address CA11	High	Low	0	R/W
	D2	ANDCA10	AND FLASH column address CA10	High	Low	0	R/W
	D1	ANDCA9	AND FLASH column address CA9	High	Low	0	R/W
	D0	ANDCA8	AND FLASH column address CA8	High	Low	0	R/W

Secure Digital (SD) / MMC Memory Card control registers

Address	Bit	Name	Function	1		0		SR	R/W
0x1860 SD card	D7	SOP	Start operation	R	Running	R	Idle	0	R/W
				W	Start	W	None	0	R/W
	D6	STOP	Stop operation	Stop		None		0	W
	D5	GNR	Get Next Response (Only for Command R136 Bits Mode)	Get Next Response		None		0	W
	D4	COM	Command Operation Mode	11: R136-Bit Mode 10:Normal Mode		01: No Response 00: No Action		0	R/W
	D3							0	R/W
	D2	BM	Bit Mode	4 Bits Mode		1 Bit Mode		0	R/W
	D1	DOM	Data operation Mode	11: Write Data 10: Read Data		0x: No Action		0	R/W
	D0							0	R/W
0x1861 SD card	D7	RIF	SD response interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D6	BRIF	SD block read finished interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D5	BWIF	SD block write finished interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D4	OBRWIF0	SD one byte R/W finished interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D3	CRCE	Status: CRC7 error	Yes		No		0	R
	D2	BWUS	Status: CRC16 error	Yes		No		0	R
	D1	FE	Status: block write unsuccessful	Yes		No		0	R
	D0	IM	SD interrupt mask register	Enable		Mask		0	R/W
0x1862 SD card	D7	SDAM	Access Method	By hardware		By CPU		0	R/W
	D6	CLKS	SD Clock Select	000 : clock/2 001 : clock/4 010 : clock/8 011 : clock/16		100 : clock/32 101 : clock/64 110 : clock/128 111 : clock/256		0	R/W
	D5							0	R/W
	D4							0	R/W
	D3	BKL	Read/Write Block Length	Block Length = 2^BKL BKL = 0 ~ 11				0	R/W
	D2							0	R/W
	D1							0	R/W
	D0							0	R/W
0x1863 SD card	D7	SDCMD47	Write: Command Bit 47 ~ 40 Read: Response Bit 47 ~ 40 (Normal Mode) Response Bit 135 ~ 128, 95 ~ 88, 55 ~ 48 (R136 Bits Mode)	High		Low		0	R/W
	D6	SDCMD46		High		Low		0	R/W
	D5	SDCMD45		High		Low		0	R/W
	D4	SDCMD44		High		Low		0	R/W
	D3	SDCMD43		High		Low		0	R/W
	D2	SDCMD42		High		Low		0	R/W
	D1	SDCMD41		High		Low		0	R/W
	D0	SDCMD40		High		Low		0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x1864 SD card	D7	SDCMD39	Write: Command Bit 39 ~ 32 Read: Response Bit 39 ~ 32 (Normal Mode) Response Bit 127 ~ 120, 87 ~ 80, 47 ~ 40 (R136 Bits Mode)	High	Low	0	R/W
	D6	SDCMD38		High	Low	0	R/W
	D5	SDCMD37		High	Low	0	R/W
	D4	SDCMD36		High	Low	0	R/W
	D3	SDCMD35		High	Low	0	R/W
	D2	SDCMD34		High	Low	0	R/W
	D1	SDCMD33		High	Low	0	R/W
	D0	SDCMD32		High	Low	0	R/W
0x1865 SD card	D7	SDCMD31	Write: Command Bit 31 ~ 24 Read: Response Bit 31 ~ 24 (Normal Mode) Response Bit 119 ~ 112, 79 ~ 72, 39 ~ 32 (R136 Bits Mode)	High	Low	0	R/W
	D6	SDCMD30		High	Low	0	R/W
	D5	SDCMD29		High	Low	0	R/W
	D4	SDCMD28		High	Low	0	R/W
	D3	SDCMD27		High	Low	0	R/W
	D2	SDCMD26		High	Low	0	R/W
	D1	SDCMD25		High	Low	0	R/W
	D0	SDCMD24		High	Low	0	R/W
0x1866 SD card	D7	SDCMD23	Write: Command Bit 23 ~ 16 Read: Response Bit 23 ~ 16 (Normal Mode) Response Bit 111 ~ 104, 71 ~ 64, 31 ~ 24 (R136 Bits Mode)	High	Low	0	R/W
	D6	SDCMD22		High	Low	0	R/W
	D5	SDCMD21		High	Low	0	R/W
	D4	SDCMD20		High	Low	0	R/W
	D3	SDCMD19		High	Low	0	R/W
	D2	SDCMD18		High	Low	0	R/W
	D1	SDCMD17		High	Low	0	R/W
	D0	SDCMD16		High	Low	0	R/W
0x1867 SD card	D7	SDCMD15	Write: Command Bit 15 ~8 Read: Response Bit 15 ~ 8 (Normal Mode) Response Bit 103 ~ 96, 63 ~ 56, 23 ~ 16, 15 ~ 8 (R136 Bits Mode)	High	Low	0	R/W
	D6	SDCMD14		High	Low	0	R/W
	D5	SDCMD13		High	Low	0	R/W
	D4	SDCMD12		High	Low	0	R/W
	D3	SDCMD11		High	Low	0	R/W
	D2	SDCMD10		High	Low	0	R/W
	D1	SDCMD09		High	Low	0	R/W
	D0	SDCMD08		High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x1868 SD card	D7	SDRWB7	Data Read/Write Buffer	High	Low	0	R/W
	D6	SDRWB6		High	Low	0	R/W
	D5	SDRWB5		High	Low	0	R/W
	D4	SDRWB4		High	Low	0	R/W
	D3	SDRWB3		High	Low	0	R/W
	D2	SDRWB2		High	Low	0	R/W
	D1	SDRWB1		High	Low	0	R/W
	D0	SDRWB0		High	Low	0	R/W
0x1869 SD card	D7						
	D6						
	D5						
	D4						
	D3						
	D2						
	D1	SDWUNB	Wait Until Not Busy (Only for R1b)	Wait	No	0	W
	D0	SDBUSY	Busy Flag (DATA 0)	Not Busy	Busy	1	R

Serial Peripheral Interface (SPI)

Address	Bit	Name	Function	1	0	SR	R/W
0x1880 SPI	D7	SPID7	SPI transmit/receive data bit 7	High	Low	0	R/W
	D6	SPID6	SPI transmit/receive data bit 6	High	Low	0	R/W
	D5	SPID5	SPI transmit/receive data bit 5	High	Low	0	R/W
	D4	SPID4	SPI transmit/receive data bit 4	High	Low	0	R/W
	D3	SPID3	SPI transmit/receive data bit 3	High	Low	0	R/W
	D2	SPID2	SPI transmit/receive data bit 2	High	Low	0	R/W
	D1	SPID1	SPI transmit/receive data bit 1	High	Low	0	R/W
	D0	SPID0	SPI transmit/receive data bit 0	High	Low	0	R/W
0x1881 SPI	D7	SPID15	SPI transmit/receive data bit 15	High	Low	0	R/W
	D6	SPID14	SPI transmit/receive data bit 14	High	Low	0	R/W
	D5	SPID13	SPI transmit/receive data bit 13	High	Low	0	R/W
	D4	SPID12	SPI transmit/receive data bit 12	High	Low	0	R/W
	D3	SPID11	SPI transmit/receive data bit 11	High	Low	0	R/W
	D2	SPID10	SPI transmit/receive data bit 10	High	Low	0	R/W
	D1	SPID9	SPI transmit/receive data bit 9	High	Low	0	R/W
	D0	SPID8	SPI transmit/receive data bit 8	High	Low	0	R/W
0x1882 SPI	D7	SPID23	SPI transmit/receive data bit 23	High	Low	0	R/W
	D6	SPID22	SPI transmit/receive data bit 22	High	Low	0	R/W
	D5	SPID21	SPI transmit/receive data bit 21	High	Low	0	R/W
	D4	SPID20	SPI transmit/receive data bit 20	High	Low	0	R/W
	D3	SPID19	SPI transmit/receive data bit 19	High	Low	0	R/W
	D2	SPID18	SPI transmit/receive data bit 18	High	Low	0	R/W
	D1	SPID17	SPI transmit/receive data bit 17	High	Low	0	R/W
	D0	SPID16	SPI transmit/receive data bit 16	High	Low	0	R/W
0x1883 SPI	D7	SPID31	SPI transmit/receive data bit 31	High	Low	0	R/W
	D6	SPID30	SPI transmit/receive data bit 30	High	Low	0	R/W
	D5	SPID29	SPI transmit/receive data bit 29	High	Low	0	R/W
	D4	SPID28	SPI transmit/receive data bit 28	High	Low	0	R/W
	D3	SPID27	SPI transmit/receive data bit 27	High	Low	0	R/W
	D2	SPID26	SPI transmit/receive data bit 26	High	Low	0	R/W
	D1	SPID25	SPI transmit/receive data bit 25	High	Low	0	R/W
	D0	SPID24	SPI transmit/receive data bit 24	High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x1884 SPI	D7						
	D6	SPICLK	SPI clock initial level select	High level	Low level	0	R/W
	D5	SPICR	Check Ready to start	Yes	No	1	R/W
	D4	SPIRUN	SPI transfer start indication	R Doing W Start	R Over W None	0	R/W
	D3	SPITMD1	Select which nibble to transmit first	Highest	Lowest	0	R/W
	D2	SPITMD0	Select which bit to transmit first	MSB	LSB	0	R/W
	D1	SPIRMD1	Select which nibble to store first	Highest	Lowest	0	R/W
	D0	SPIRMD0	Select which bit to store first	MSB	LSB	0	R/W
0x1885 SPI	D7	SPIF	SPI interrupt factor flag	R Yes W Reset	R No W None	0	R/W
	D6	SPIM	SPI interrupt mask register	Enable	Mask	0	R/W
	D5	SPISIZE1	SPI data length select	11: 32bits 10:24bits	01:16bits 00:8bits	1	R/W
	D4	SPISIZE0				1	R/W
	D3	SPICK3	SPI clock frequency select	Select range n = 0 ~ 12 SPICLK = CPU clock / 2 ^(n+1) For instance, n=4 SPICLK = CPU clock / 32		0	R/W
	D2	SPICK2				0	R/W
	D1	SPICK1				1	R/W
	D0	SPICK0				0	R/W

Universal Serial Bus (USB) Interface control registers

Address	Bit	Name	Function	1	0	SR	R/W
0x1890 USB	D7	USBSHK	USB handshake status	ACK	NACK	0	R
	D6	BFFUL	Buffer full	Full	Not Full	0	R
	D5	BFEMP	Buffer empty	Empty	Not Empty	1	R
	D4	MS_RST	Mass Storage Reset	Reset (R)	Clear (R/W)	0	R/W
	D3	BOTEN	Enable BOT protocol	Enable	Disable	0	R/W
	D2	FCSW	Force into CSW	Enable	Disable	0	R/W
	D1	STALL	USB pipe stall	1	0	0	R/W
	D0	USB_GO	USB ready to go	Start	None	0	R/W
0x1891 USB	D7	FCBW	interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D6	FDIN	interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D5	FDOUT	interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D4	FCSW	interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D3	ECBW	interrupt mask register	Enable	Mask	0	R/W
	D2	EDIN	interrupt mask register	Enable	Mask	0	R/W
	D1	EDOUT	interrupt mask register	Enable	Mask	0	R/W
	D0	ECSW	interrupt mask register	Enable	Mask	0	R/W
0x1892 USB	D7	MLUM3	Maximum Logical Unit Number	High	Low	0	R/W
	D6	MLUN2		High	Low		
	D5	MLUN1		High	Low		
	D4	MLUN0		High	Low		
	D3	SUSEN	USB suspend enable	Enable	Disable	0	R/W
	D2	BTIPORT	Block Transfer Port	Enable	Disable	0	R/W
	D1	WBPRST	Write Buffer pointer reset	Reset	None	0	W
	D0	RBPRST	Read Buffer pointer reset	Reset	None	0	W
0x1893 USB	D7	USBD7	USB R/W Buffer (Buffer Length =64 Bytes)	High	Low	0	R/W
	D6	USBD6		High	Low	0	R/W
	D5	USBD5		High	Low	0	R/W
	D4	USBD4		High	Low	0	R/W
	D3	USBD3		High	Low	0	R/W
	D2	USBD2		High	Low	0	R/W
	D1	USBD1		High	Low	0	R/W
	D0	USBD0		High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x1894 USB	D7	USBVID7	Vender ID Bit 7 ~ 0	High	Low	0	R/W
	D6	USBVID6		High	Low	0	R/W
	D5	USBVID5		High	Low	1	R/W
	D4	USBVID4		High	Low	0	R/W
	D3	USBVID3		High	Low	1	R/W
	D2	USBVID2		High	Low	0	R/W
	D1	USBVID1		High	Low	1	R/W
	D0	USBVID0		High	Low	0	R/W
0x1895 USB	D7	USBVID15	Vender ID Bit 15 ~ 8	High	Low	0	R/W
	D6	USBVID14		High	Low	0	R/W
	D5	USBVID13		High	Low	0	R/W
	D4	USBVID12		High	Low	0	R/W
	D3	USBVID11		High	Low	0	R/W
	D2	USBVID10		High	Low	1	R/W
	D1	USBVID9		High	Low	1	R/W
	D0	USBVID8		High	Low	0	R/W
0x1896 USB	D7	MAXCUR7	Maximum Current Bit 7 ~ 0 (in unit of 2 mA)	High	Low	0	R/W
	D6	MAXCUR6		High	Low	0	R/W
	D5	MAXCUR5		High	Low	1	R/W
	D4	MAXCUR4		High	Low	1	R/W
	D3	MAXCUR3		High	Low	0	R/W
	D2	MAXCUR2		High	Low	0	R/W
	D1	MAXCUR1		High	Low	1	R/W
	D0	MAXCUR0		High	Low	0	R/W
0x1898 USB	D7	SNUM0_7	Serial Number Byte 0	High	Low	0	R/W
	D6	SNUM0_6		High	Low	0	R/W
	D5	SNUM0_5		High	Low	1	R/W
	D4	SNUM0_4		High	Low	1	R/W
	D3	SNUM0_3		High	Low	0	R/W
	D2	SNUM0_2		High	Low	0	R/W
	D1	SNUM0_1		High	Low	0	R/W
	D0	SNUM0_0		High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x1899 USB	D7	SNUM1_7	Serial Number Byte 1	High	Low	0	R/W
	D6	SNUM1_6		High	Low	0	R/W
	D5	SNUM1_5		High	Low	1	R/W
	D4	SNUM1_4		High	Low	1	R/W
	D3	SNUM1_3		High	Low	0	R/W
	D2	SNUM1_2		High	Low	0	R/W
	D1	SNUM1_1		High	Low	0	R/W
	D0	SNUM1_0		High	Low	1	R/W
0x189A USB	D7	SNUM2_7	Serial Number Byte 2	High	Low	0	R/W
	D6	SNUM2_6		High	Low	1	R/W
	D5	SNUM2_5		High	Low	0	R/W
	D4	SNUM2_4		High	Low	0	R/W
	D3	SNUM2_3		High	Low	0	R/W
	D2	SNUM2_2		High	Low	0	R/W
	D1	SNUM2_1		High	Low	0	R/W
	D0	SNUM2_0		High	Low	1	R/W
0x189B USB	D7	SNUM3_7	Serial Number Byte 3	High	Low	0	R/W
	D6	SNUM3_6		High	Low	1	R/W
	D5	SNUM3_5		High	Low	0	R/W
	D4	SNUM3_4		High	Low	0	R/W
	D3	SNUM3_3		High	Low	0	R/W
	D2	SNUM3_2		High	Low	0	R/W
	D1	SNUM3_1		High	Low	0	R/W
	D0	SNUM3_0		High	Low	1	R/W
0x189C USB	D7	SNUM4_7	Data In Transfer Length	High	Low	0	R/W
	D6	SNUM4_6		High	Low	1	R/W
	D5	SNUM4_5		High	Low	0	R/W
	D4	SNUM4_4		High	Low	0	R/W
	D3	SNUM4_3		High	Low	0	R/W
	D2	SNUM4_2		High	Low	0	R/W
	D1	SNUM4_1		High	Low	0	R/W
	D0	SNUM4_0		High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x189D USB	D7	SNUM5_7	Data In USB Transfer Length	High	Low	0	R
	D6	SNUM5_6		High	Low	0	R
	D5	SNUM5_5		High	Low	0	R
	D4	SNUM5_4		High	Low	0	R
	D3	SNUM5_3		High	Low	0	R
	D2	SNUM5_2		High	Low	0	R
	D1	SNUM5_1		High	Low	0	R
	D0	SNUM5_0		High	Low	0	R
0x189E USB	D7	SNUM6_7	Data Out Transfer Length	High	Low	0	R/W
	D6	SNUM6_6		High	Low	1	R/W
	D5	SNUM6_5		High	Low	0	R/W
	D4	SNUM6_4		High	Low	0	R/W
	D3	SNUM6_3		High	Low	0	R/W
	D2	SNUM6_2		High	Low	0	R/W
	D1	SNUM6_1		High	Low	0	R/W
	D0	SNUM6_0		High	Low	0	R/W
0x189F USB	D7	SNUM7_7	Data Out USB Transfer Length	High	Low	0	R
	D6	SNUM7_6		High	Low	0	R
	D5	SNUM7_5		High	Low	0	R
	D4	SNUM7_4		High	Low	0	R
	D3	SNUM7_3		High	Low	0	R
	D2	SNUM7_2		High	Low	0	R
	D1	SNUM7_1		High	Low	0	R
	D0	SNUM7_0		High	Low	0	R

Address	Bit	Name	Function	1	0	SR	R/W
0x1870 USB	D7	USBPID7	Product ID Bit 7 ~ 0	High	Low	0	R/W
	D6	USBPID6		High	Low	0	R/W
	D5	USBPID5		High	Low	0	R/W
	D4	USBPID4		High	Low	1	R/W
	D3	USBPID3		High	Low	1	R/W
	D2	USBPID2		High	Low	0	R/W
	D1	USBPID1		High	Low	0	R/W
	D0	USBPID0		High	Low	0	R/W
0x1871 USB	D7	USBVPD15	Product ID Bit 15 ~ 8	High	Low	0	R/W
	D6	USBVPD14		High	Low	1	R/W
	D5	USBVPD13		High	Low	1	R/W
	D4	USBVPD12		High	Low	0	R/W
	D3	USBVPD11		High	Low	0	R/W
	D2	USBVPD10		High	Low	1	R/W
	D1	USBPID9		High	Low	1	R/W
	D0	USBPID8		High	Low	0	R/W

32/16 unsigned divider

Address	Bit	Name	Function	1	0	SR	R/W
0x18A0 Divide Register	D7	DIVID7	Dividend data 7/ Quotient 7	High	Low	0	R/W
	D6	DIVID6	Dividend data 6/ Quotient 6	High	Low	0	R/W
	D5	DIVID5	Dividend data 5/ Quotient 5	High	Low	0	R/W
	D4	DIVID4	Dividend data 4/ Quotient 4	High	Low	0	R/W
	D3	DIVID3	Dividend data 3/ Quotient 3	High	Low	0	R/W
	D2	DIVID2	Dividend data 2/ Quotient 2	High	Low	0	R/W
	D1	DIVID1	Dividend data 1/ Quotient 1	High	Low	0	R/W
	D0	DIVID0	Dividend data 0/ Quotient 0	High	Low	0	R/W
0x18A1 Divide Register	D7	DIVID15	Dividend data 15/ Quotient 15	High	Low	0	R/W
	D6	DIVID14	Dividend data 14/ Quotient 14	High	Low	0	R/W
	D5	DIVID13	Dividend data 13/ Quotient 13	High	Low	0	R/W
	D4	DIVID12	Dividend data 12/ Quotient 12	High	Low	0	R/W
	D3	DIVID11	Dividend data 11/ Quotient 11	High	Low	0	R/W
	D2	DIVID10	Dividend data 10/ Quotient 10	High	Low	0	R/W
	D1	DIVID9	Dividend data 9/ Quotient 9	High	Low	0	R/W
	D0	DIVID8	Dividend data 8/ Quotient 8	High	Low	0	R/W
0x18A2 Divide Register	D7	DIVID23	Dividend data 23/ Remainder 15	High	Low	0	R/W
	D6	DIVID22	Dividend data 22/ Remainder 14	High	Low	0	R/W
	D5	DIVID21	Dividend data 21/ Remainder 13	High	Low	0	R/W
	D4	DIVID20	Dividend data 20/ Remainder 12	High	Low	0	R/W
	D3	DIVID19	Dividend data 19/ Remainder 11	High	Low	0	R/W
	D2	DIVID18	Dividend data 18/ Remainder 10	High	Low	0	R/W
	D1	DIVID17	Dividend data 17/ Remainder 9	High	Low	0	R/W
	D0	DIVID16	Dividend data 16/ Remainder 8	High	Low	0	R/W
0x18A3 Divide Register	D7	DIVID31	Dividend data 31/ Remainder 7	High	Low	0	R/W
	D6	DIVID30	Dividend data 30/ Remainder 6	High	Low	0	R/W
	D5	DIVID29	Dividend data 29/ Remainder 5	High	Low	0	R/W
	D4	DIVID28	Dividend data 28/ Remainder 4	High	Low	0	R/W
	D3	DIVID27	Dividend data 27/ Remainder 3	High	Low	0	R/W
	D2	DIVID26	Dividend data 26/ Remainder 2	High	Low	0	R/W
	D1	DIVID25	Dividend data 25/ Remainder 1	High	Low	0	R/W
	D0	DIVID24	Dividend data 24/ Remainder 0	High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x18A4 Divide Register	D7	DIVIS7	Divisor data 7	High	Low	0	W
	D6	DIVID6	Divisor data 6	High	Low	0	W
	D5	DIVID5	Divisor data 5	High	Low	0	W
	D4	DIVID4	Divisor data 4	High	Low	0	W
	D3	DIVID3	Divisor data 3	High	Low	0	W
	D2	DIVID2	Divisor data 2	High	Low	0	W
	D1	DIVID1	Divisor data 1	High	Low	0	W
	D0	DIVID0	Divisor data 0	High	Low	0	W
0x18A5 Divide Register	D7	DIVID15	Divisor data 15	High	Low	0	W
	D6	DIVID14	Divisor data 14	High	Low	0	W
	D5	DIVID13	Divisor data 13	High	Low	0	W
	D4	DIVID12	Divisor data 12	High	Low	0	W
	D3	DIVID11	Divisor data 11	High	Low	0	W
	D2	DIVID10	Divisor data 10	High	Low	0	W
	D1	DIVID9	Divisor data 9	High	Low	0	W
	D0	DIVID8	Divisor data 8	High	Low	0	W
0x18A6 Divide Register	D7						
	D6						
	D5						
	D4						
	D3						
	D2						
	D1	DFF	Divider finish flag	R Yes W Reset	R No W None	0	R/W
	D0						

16x16 unsigned multiplication

Address	Bit	Name	Function	1	0	SR	R/W
0x18A8 Multiply Register	D7	MCAND7	Multiplicand data 7/ Product 7	High	Low	0	R/W
	D6	MCAND6	Multiplicand data 6/ Product 6	High	Low	0	R/W
	D5	MCAND5	Multiplicand data 5/ Product 5	High	Low	0	R/W
	D4	MCAND4	Multiplicand data 4/ Product 4	High	Low	0	R/W
	D3	MCAND3	Multiplicand data 3/ Product 3	High	Low	0	R/W
	D2	MCAND2	Multiplicand data 2/ Product 2	High	Low	0	R/W
	D1	MCAND1	Multiplicand data 1/ Product 1	High	Low	0	R/W
	D0	MCAND0	Multiplicand data 0/ Product 0	High	Low	0	R/W
0x18A9 Multiply Register	D7	MCAND15	Multiplicand data 15/ Product 15	High	Low	0	R/W
	D6	MCAND14	Multiplicand data 14/ Product 14	High	Low	0	R/W
	D5	MCAND13	Multiplicand data 13/ Product 13	High	Low	0	R/W
	D4	MCAND12	Multiplicand data 12/ Product 12	High	Low	0	R/W
	D3	MCAND11	Multiplicand data 11/ Product 11	High	Low	0	R/W
	D2	MCAND10	Multiplicand data 10/ Product 10	High	Low	0	R/W
	D1	MCAND9	Multiplicand data 9/ Product 9	High	Low	0	R/W
	D0	MCAND8	Multiplicand data 8/ Product 8	High	Low	0	R/W
0x18AA Multiply Register	D7	MIER7	Multiplier data 7/ Product 23	High	Low	0	R/W
	D6	MIER6	Multiplier data 6/ Product 22	High	Low	0	R/W
	D5	MIER5	Multiplier data 5/ Product 21	High	Low	0	R/W
	D4	MIER4	Multiplier data 4/ Product 20	High	Low	0	R/W
	D3	MIER3	Multiplier data 3/ Product 19	High	Low	0	R/W
	D2	MIER2	Multiplier data 2/ Product 18	High	Low	0	R/W
	D1	MIER1	Multiplier data 1/ Product 17	High	Low	0	R/W
	D0	MIER0	Multiplier data 0/ Product 16	High	Low	0	R/W
0x18AB Multiply Register	D7	MIER15	Multiplier data 15/ Product 31	High	Low	0	R/W
	D6	MIER14	Multiplier data 14/ Product 30	High	Low	0	R/W
	D5	MIER13	Multiplier data 13/ Product 29	High	Low	0	R/W
	D4	MIER12	Multiplier data 12/ Product 28	High	Low	0	R/W
	D3	MIER11	Multiplier data 11/ Product 27	High	Low	0	R/W
	D2	MIER10	Multiplier data 10/ Product 26	High	Low	0	R/W
	D1	MIER9	Multiplier data 9/ Product 25	High	Low	0	R/W
	D0	MIER8	Multiplier data 8/ Product 24	High	Low	0	R/W

Address	Bit	Name	Function	1		0		SR	R/W
0x18AC Multiply Register	D7								
	D6								
	D5								
	D4								
	D3								
	D2								
	D1	MULTF	Multiplication finish flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D0								

Data Rearrangement registers

Address	Bit	Name	Function	1	0	SR	R/W
0x18B0 DR Register	D7	DRD7	DR Write Data 7/ DR Read Data 31	High	Low	0	R/W
	D6	DRD6	DR Write Data 6/ DR Read Data 30	High	Low	0	R/W
	D5	DRD5	DR Write Data 5/ DR Read Data 29	High	Low	0	R/W
	D4	DRD4	DR Write Data 4/ DR Read Data 28	High	Low	0	R/W
	D3	DRD3	DR Write Data 3/ DR Read Data 27	High	Low	0	R/W
	D2	DRD2	DR Write Data 2/ DR Read Data 26	High	Low	0	R/W
	D1	DRD1	DR Write Data 1/ DR Read Data 25	High	Low	0	R/W
	D0	DRD0	DR Write Data 0/ DR Read Data 24	High	Low	0	R/W
0x18B1 DR Register	D7	DRD15	DR Write Data 15/ DR Read Data 23	High	Low	0	R/W
	D6	DRD14	DR Write Data 14/ DR Read Data 22	High	Low	0	R/W
	D5	DRD13	DR Write Data 13/ DR Read Data 21	High	Low	0	R/W
	D4	DRD12	DR Write Data 12/ DR Read Data 20	High	Low	0	R/W
	D3	DRD11	DR Write Data 11/ DR Read Data 19	High	Low	0	R/W
	D2	DRD10	DR Write Data 10/ DR Read Data 18	High	Low	0	R/W
	D1	DRD9	DR Write Data 9/ DR Read Data 17	High	Low	0	R/W
	D0	DRD8	DR Write Data 8/ DR Read Data 16	High	Low	0	R/W
0x18B2 DR Register	D7	DRD23	DR Write Data 23/ DR Read Data 15	High	Low	0	R/W
	D6	DRD22	DR Write Data 22/ DR Read Data 14	High	Low	0	R/W
	D5	DRD21	DR Write Data 21/ DR Read Data 13	High	Low	0	R/W
	D4	DRD20	DR Write Data 20/ DR Read Data 12	High	Low	0	R/W
	D3	DRD19	DR Write Data 19/ DR Read Data 11	High	Low	0	R/W
	D2	DRD18	DR Write Data 18/ DR Read Data 10	High	Low	0	R/W
	D1	DRD17	DR Write Data 17/ DR Read Data 9	High	Low	0	R/W
	D0	DRD16	DR Write Data 16/ DR Read Data 8	High	Low	0	R/W
0x18B3 DR Register	D7	DRD31	DR Write Data 31/ DR Read Data 7	High	Low	0	R/W
	D6	DRD30	DR Write Data 30/ DR Read Data 6	High	Low	0	R/W
	D5	DRD29	DR Write Data 29/ DR Read Data 5	High	Low	0	R/W
	D4	DRD28	DR Write Data 28/ DR Read Data 4	High	Low	0	R/W
	D3	DRD27	DR Write Data 27/ DR Read Data 3	High	Low	0	R/W
	D2	DRD26	DR Write Data 26/ DR Read Data 2	High	Low	0	R/W
	D1	DRD25	DR Write Data 25/ DR Read Data 1	High	Low	0	R/W
	D0	DRD24	DR Write Data 24/ DR Read Data 0	High	Low	0	R/W

Parity Check registers

Address	Bit	Name	Function	1	0	SR	R/W
0x18B4 MIS	D7	PCD7	Parity Check Data7	High	Low	0	W
	D6	PCD6	Parity Check Data6	High	Low	0	W
	D5	PCD5	Parity Check Data5	High	Low	0	W
	D4	PCD4	Parity Check Data4	High	Low	0	W
	D3	PCD3	Parity Check Data3	High	Low	0	W
	D2	PCD2	Parity Check Data2	High	Low	0	W
	D1	PCD1	Parity Check Data1	High	Low	0	W
	D0	PCD0	Parity Check Data0	High	Low	0	W
0x18B5 MIS	D7						
	D6						
	D5						
	D4						
	D3						
	D2						
	D1						
	D0	PCB	Parity Check Bit	High	Low	0	R/W

DMA control registers

Address	Bit	Name	Function	1	0	SR	R/W
0x18C0 DMA Register	D7						
	D6						
	D5						
	D4						
	D3						
	D2	DMAEN	DMA enable	Enable	Disable	0	R/W
	D1	DMADIR	DMA direction	Ram to Flash	Flash to Ram	0	R/W
	D0	DMAGO	DMA start trigger	R Busy W Trigger	R Ready W None	0	R/W
0x18C1 DMA Register	D7						
	D6						
	D5						
	D4						
	D3						
	D2						
	D1	IDMA	DMA finish interrupt factor flag	R Yes W Reset	R No W None	0	R/W
	D0	EIDMA	DMA interrupt mask register	Enable	Mask	0	R/W
0x18C2 DMA Register	D7	DMAA[7]	The RAM Start Address for DMA	DMAA[12:0] = 0x0000-17FF		00	R/W
	D6	DMAA[6]					
	D5	DMAA[5]					
	D4	DMAA[4]					
	D3	DMAA[3]					
	D2	DMAA[2]					
	D1	DMAA[1]					
	D0	DMAA[0]					
0x18C3 DMA Register	D7						
	D6						
	D5						
	D4	DMAA[12]	The RAM Start Address for DMA	DMAA[12:0] = 0x0000-17FF		0	R/W
	D3	DMAA[11]					
	D2	DMAA[10]					
	D1	DMAA[9]					
	D0	DMAA[8]					

Debug registers

Address	Bit	Name	Function	1	0	SR	R/W
0x18C4 Debug Register	D7						
	D6						
	D5						
	D4						
	D3						
	D2						
	D1	NMIB_stop	Stop NMIB Interrupt	Stop	None	0	W
	D0	NMIB_EN	Enable Debug Mode	Enable	Disable	0	R/W
0x18C5 Debug Register	D7						
	D6						
	D5						
	D4	EN4	Enable 0x18CE & 0x18CF	Enable	Disable	0	R/W
	D3	EN3	Enable 0x18CC & 0x18CD	Enable	Disable	0	R/W
	D2	EN2	Enable 0x18CA & 0x18CB	Enable	Disable	0	R/W
	D1	EN1	Enable 0x18C8 & 0x18C9	Enable	Disable	0	R/W
	D0	EN0	Enable 0x18C6 & 0x18C7	Enable	Disable	0	R/W
0x18C6 Debug Register	D7	ADDR0_L[7]	Debug Address “0” low byte	High	Low	0	R/W
	D6	ADDR0_L[6]	Debug Address “0” low byte	High	Low	0	R/W
	D5	ADDR0_L[5]	Debug Address “0” low byte	High	Low	0	R/W
	D4	ADDR0_L[4]	Debug Address “0” low byte	High	Low	0	R/W
	D3	ADDR0_L[3]	Debug Address “0” low byte	High	Low	0	R/W
	D2	ADDR0_L[2]	Debug Address “0” low byte	High	Low	0	R/W
	D1	ADDR0_L[1]	Debug Address “0” low byte	High	Low	0	R/W
	D0	ADDR0_L[0]	Debug Address “0” low byte	High	Low	0	R/W
0x18C7 Debug Register	D7	ADDR0_H[7]	Debug Address “0” high byte	High	Low	0	R/W
	D6	ADDR0_H[6]	Debug Address “0” high byte	High	Low	0	R/W
	D5	ADDR0_H[5]	Debug Address “0” high byte	High	Low	0	R/W
	D4	ADDR0_H[4]	Debug Address “0” high byte	High	Low	0	R/W
	D3	ADDR0_H[3]	Debug Address “0” high byte	High	Low	0	R/W
	D2	ADDR0_H[2]	Debug Address “0” high byte	High	Low	0	R/W
	D1	ADDR0_H[1]	Debug Address “0” high byte	High	Low	0	R/W
	D0	ADDR0_H[0]	Debug Address “0” high byte	High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x18C8 Debug Register	D7	ADDR1_L[7]	Debug Address “1” low byte	High	Low	0	R/W
	D6	ADDR1_L[6]	Debug Address “1” low byte	High	Low	0	R/W
	D5	ADDR1_L[5]	Debug Address “1” low byte	High	Low	0	R/W
	D4	ADDR1_L[4]	Debug Address “1” low byte	High	Low	0	R/W
	D3	ADDR1_L[3]	Debug Address “1” low byte	High	Low	0	R/W
	D2	ADDR1_L[2]	Debug Address “1” low byte	High	Low	0	R/W
	D1	ADDR1_L[1]	Debug Address “1” low byte	High	Low	0	R/W
	D0	ADDR1_L[0]	Debug Address “1” low byte	High	Low	0	R/W
0x18C9 Debug Register	D7	ADDR1_H[7]	Debug Address “1” high byte	High	Low	0	R/W
	D6	ADDR1_H[6]	Debug Address “1” high byte	High	Low	0	R/W
	D5	ADDR1_H[5]	Debug Address “1” high byte	High	Low	0	R/W
	D4	ADDR1_H[4]	Debug Address “1” high byte	High	Low	0	R/W
	D3	ADDR1_H[3]	Debug Address “1” high byte	High	Low	0	R/W
	D2	ADDR1_H[2]	Debug Address “1” high byte	High	Low	0	R/W
	D1	ADDR1_H[1]	Debug Address “1” high byte	High	Low	0	R/W
	D0	ADDR1_H[0]	Debug Address “1” high byte	High	Low	0	R/W
0x18CA Debug Register	D7	ADDR2_L[7]	Debug Address “2” low byte	High	Low	0	R/W
	D6	ADDR2_L[6]	Debug Address “2” low byte	High	Low	0	R/W
	D5	ADDR2_L[5]	Debug Address “2” low byte	High	Low	0	R/W
	D4	ADDR2_L[4]	Debug Address “2” low byte	High	Low	0	R/W
	D3	ADDR2_L[3]	Debug Address “2” low byte	High	Low	0	R/W
	D2	ADDR2_L[2]	Debug Address “2” low byte	High	Low	0	R/W
	D1	ADDR2_L[1]	Debug Address “2” low byte	High	Low	0	R/W
	D0	ADDR2_L[0]	Debug Address “2” low byte	High	Low	0	R/W
0x18CB Debug Register	D7	ADDR2_H[7]	Debug Address “2” high byte	High	Low	0	R/W
	D6	ADDR2_H[6]	Debug Address “2” high byte	High	Low	0	R/W
	D5	ADDR2_H[5]	Debug Address “2” high byte	High	Low	0	R/W
	D4	ADDR2_H[4]	Debug Address “2” high byte	High	Low	0	R/W
	D3	ADDR2_H[3]	Debug Address “2” high byte	High	Low	0	R/W
	D2	ADDR2_H[2]	Debug Address “2” high byte	High	Low	0	R/W
	D1	ADDR2_H[1]	Debug Address “2” high byte	High	Low	0	R/W
	D0	ADDR2_H[0]	Debug Address “2” high byte	High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x18CC Debug Register	D7	ADDR3_L[7]	Debug Address “3” low byte	High	Low	0	R/W
	D6	ADDR3_L[6]	Debug Address “3” low byte	High	Low	0	R/W
	D5	ADDR3_L[5]	Debug Address “3” low byte	High	Low	0	R/W
	D4	ADDR3_L[4]	Debug Address “3” low byte	High	Low	0	R/W
	D3	ADDR3_L[3]	Debug Address “3” low byte	High	Low	0	R/W
	D2	ADDR3_L[2]	Debug Address “3” low byte	High	Low	0	R/W
	D1	ADDR3_L[1]	Debug Address “3” low byte	High	Low	0	R/W
	D0	ADDR3_L[0]	Debug Address “3” low byte	High	Low	0	R/W
0x18CD Debug Register	D7	ADDR3_H[7]	Debug Address “3” high byte	High	Low	0	R/W
	D6	ADDR3_H[6]	Debug Address “3” high byte	High	Low	0	R/W
	D5	ADDR3_H[5]	Debug Address “3” high byte	High	Low	0	R/W
	D4	ADDR3_H[4]	Debug Address “3” high byte	High	Low	0	R/W
	D3	ADDR3_H[3]	Debug Address “3” high byte	High	Low	0	R/W
	D2	ADDR3_H[2]	Debug Address “3” high byte	High	Low	0	R/W
	D1	ADDR3_H[1]	Debug Address “3” high byte	High	Low	0	R/W
	D0	ADDR3_H[0]	Debug Address “3” high byte	High	Low	0	R/W
0x18CE Debug Register	D7	ADDR4_L[7]	Debug Address “4” low byte	High	Low	0	R/W
	D6	ADDR4_L[6]	Debug Address “4” low byte	High	Low	0	R/W
	D5	ADDR4_L[5]	Debug Address “4” low byte	High	Low	0	R/W
	D4	ADDR4_L[4]	Debug Address “4” low byte	High	Low	0	R/W
	D3	ADDR4_L[3]	Debug Address “4” low byte	High	Low	0	R/W
	D2	ADDR4_L[2]	Debug Address “4” low byte	High	Low	0	R/W
	D1	ADDR4_L[1]	Debug Address “4” low byte	High	Low	0	R/W
	D0	ADDR4_L[0]	Debug Address “4” low byte	High	Low	0	R/W
0x18CF Debug Register	D7	ADDR4_H[7]	Debug Address “4” high byte	High	Low	0	R/W
	D6	ADDR4_H[6]	Debug Address “4” high byte	High	Low	0	R/W
	D5	ADDR4_H[5]	Debug Address “4” high byte	High	Low	0	R/W
	D4	ADDR4_H[4]	Debug Address “4” high byte	High	Low	0	R/W
	D3	ADDR4_H[3]	Debug Address “4” high byte	High	Low	0	R/W
	D2	ADDR4_H[2]	Debug Address “4” high byte	High	Low	0	R/W
	D1	ADDR4_H[1]	Debug Address “4” high byte	High	Low	0	R/W
	D0	ADDR4_H[0]	Debug Address “4” high byte	High	Low	0	R/W

USBDMA control registers

Address	Bit	Name	Function	1	0	SR	R/W
0x18D0 USBDMA Register	D7						
	D6						
	D5						
	D4						
	D3	RUDMAEN	Ram and USBDMA data transfer enable	Enable	Disable	0	R/W
	D2						
	D1	DMAEN	DMA enable	Enable	Disable	0	R/W
	D0	DMAGO	DMA start trigger	R Busy / W Trigger	R Ready / W None	0	R/W
0x18D1 USBDMA Register	D7						
	D6						
	D5	IRRUDMA	Ram & USBDMA transfer finish interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D4	EIRRUDMA	Ram & USBDMA transfer interrupt mask register	Enable	Mask	0	R/W
	D3	IRDMA	Read DMA finish interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D2	EIRDMA	Read DMA interrupt mask register	Enable	Mask	0	R/W
	D1	IWDMA	Write DMA finish interrupt factor flag	R Yes / W Reset	R No / W None	0	R/W
	D0	EIWDMA	Write DMA interrupt mask register	Enable	Mask	0	R/W
0x18D2 USBDMA Register	D7						
	D6						
	D5						
	D4						
	D3	DMABL[3]	USBDMA block length	Block Length = 2^BKL BKL = 0 ~ 9 (maximum 512 bytes)		00	R/W
	D2	DMABL[2]					
	D1	DMABL[1]					
	D0	DMABL[0]					
0x18D3 USBDMA Register	D7						
	D6						
	D5						
	D4						
	D3						
	D2						
	D1	RAMTEST	Start USBDMA SRAM BIST testing	R Busy / W Trigger	R Ready / W None	0	R/W
	D0	RAMPASS	SRAM BIST testing result	Pass	No pass	1	R

Address	Bit	Name	Function	1	0	SR	R/W
0x18D4 USBDMA Register	D7						
	D6						
	D5						
	D4						
	D3	RAM0S[1]	DMA SRAM 0 status	00 : empty ; 01 : full 10 : read busy 11 : write busy		0	R
	D2	RAM0S[0]					
	D1	RAM1S[1]	DMA SRAM 1 status	00 : empty ; 01 : full 10 : read busy 11 : write busy		0	R
	D0	RAM1S[0]					
0x18D5 USBDMA Register	D7	RAMAD [7]	Address for CPU read or write RAM of USBDMA	High	Low	0	R/W
	D6	RAMAD [6]					
	D5	RAMAD [5]					
	D4	RAMAD [4]					
	D3	RAMAD [3]					
	D2	RAMAD [2]					
	D1	RAMAD [1]					
	D0	RAMAD [0]					
0x18D6 USBDMA Register	D7		Address for CPU read or write RAM of USBDMA	High	Low	0	R/W
	D6						
	D5						
	D4						
	D3						
	D2						
	D1						
	D0	RAMAD [8]					
0x18D7 USBDMA Register	D7	RAMDA [7]	Writing RAMDA is for CPU writes data to RAM Reading RAMDA is for CPU reads data from RAM	High	Low	0	R/W
	D6	RAMDA [6]					
	D5	RAMDA [5]					
	D4	RAMDA [4]					
	D3	RAMDA [3]					
	D2	RAMDA [2]					
	D1	RAMDA [1]					
	D0	RAMDA [0]					

Address	Bit	Name	Function	1	0	SR	R/W
0x18D8 USBDMA Register	D7						
	D6						
	D5						
	D4						
	D3						
	D2	SEND	Trigger cpu read or write RAM of USBDMA	Send	None	0	R/W
	D1	WR1_RD0	Select read or write RAM	Write	Read	0	R/W
	D0	A0_B1	Select RAM A or RAM B	RAM B	RAM A	0	R/W

ADC System and Interrupt Status Registers

Address	Bit	Name	Function	1	0	SR	R/W
0x18E0 ADC Register	D7						
	D6	ADCMODE	Select operating mode	One shot	Normal	0	R/W
	D5	ADSEL1	ADC channel select	00 : AD0 01 : AD1	10 : AD2 11 : AD3	0	R/W
	D4	ADSEL0				0	R/W
	D3	ADCSH	Turn on ADC using one shot	on	off	0	W
	D2	IADC	ADC interrupt	R: Yes W: Reset	R: No W: None	0	R/W
	D1	EIADC	ADC interrupt mask	enable	mask	0	R/W
	D0	ADCON	ADC on/off	on	off	0	R/W
0x18E2 ADC Register	D7	VALID	When VALID=0, ADC data is invalid and CPU should stop to read ADC data	VALID	INVALID	0	R
	D6						
	D5	CHANNEL 1	ADC channel	00 : AD0 01 : AD1	10 : AD2 11 : AD3	0	R
	D4	CHANNEL 0				0	R
	D3	ADC11	ADC output data(From buffer)	high	low	0	R
	D2	ADC10		high	low	0	R
	D1	ADC9		high	low	0	R
	D0	ADC8		high	low	0	R
0x18E3 ADC Register	D7	ADC7		high	low	0	R
	D6	ADC6		high	low	0	R
	D5	ADC5		high	low	0	R
	D4	ADC4		high	low	0	R
	D3	ADC3		high	low	0	R
	D2	ADC2		high	low	0	R
	D1	ADC1		high	low	0	R
	D0	ADC0		high	low	0	R
0x18E4 ADC Register	D7	MAX7	MAX ADC value	high	low	0	R/W
	D6	MAX6		high	low	0	R/W
	D5	MAX5		high	low	0	R/W
	D4	MAX4		high	low	0	R/W
	D3	MAX3		high	low	0	R/W
	D2	MAX2		high	low	0	R/W
	D1	MAX1		high	low	0	R/W
	D0	MAX0		high	low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x18E5 ADC Register	D7						
	D6						
	D5	XADCSH	Read ADC trigger signal	none	trigger	0	R
	D4	ADCCLK	Read ADC operation CLK	high	low	0	R
	D3	XADINT	Read ADC interrupt	none	interrupt	0	R
	D2	BUSY	ADC busy	Busy	none	0	R
	D1						
	D0						
0x18E6 ADC Register	D7	ADC11	ADC input data(From ADC)	high	low	0	R
	D6	ADC10		high	low	0	R
	D5	ADC9		high	low	0	R
	D4	ADC8		high	low	0	R
	D3	ADC7		high	low	0	R
	D2	ADC6		high	low	0	R
	D1	ADC5		high	low	0	R
	D0	ADC4		high	low	0	R
0x18E7 ADC Register	D7	ADC3	ADC input data(From ADC)	high	low	0	R
	D6	ADC2		high	low	0	R
	D5	ADC1		high	low	0	R
	D4	ADC0		high	low	0	R
	D3						
	D2						
	D1						
	D0						
0x18E8 ADC Register	D7	PREDIV7	ADC system & MP3 clock pre-divider (ADC clock = Fosc3/(PREDIV+1))	high	low	0	R/W
	D6	PREDIV6		high	low	0	R/W
	D5	PREDIV5		high	low	0	R/W
	D4	PREDIV4		high	low	0	R/W
	D3	PREDIV3		high	low	0	R/W
	D2	PREDIV2		high	low	1	R/W
	D1	PREDIV1		high	low	1	R/W
	D0	PREDIV0		high	low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x18E9 ADC Register	D7	POSTDIV7	ADC system & MP3 clock post-divider (sample rate) (sample-rate=clock/(POSTDIV+1))	high	low	0	R/W
	D6	POSTDIV6		high	low	0	R/W
	D5	POSTDIV5		high	low	0	R/W
	D4	POSTDIV4		high	low	1	R/W
	D3	POSTDIV3		high	low	1	R/W
	D2	POSTDIV2		high	low	1	R/W
	D1	POSTDIV1		high	low	1	R/W
	D0	POSTDIV0		high	low	1	R/W

Volume control registers

Address	Bit	Name	Function	1	0	SR	R/W
0x18EA Volume Control Register	D7						
	D6						
	D5						
	D4	VOL4_L	Left volume control value (0~31)	high	low	0	R/W
	D3	VOL3_L		high	low	0	R/W
	D2	VOL2_L		high	low	0	R/W
	D1	VOL1_L		high	low	0	R/W
	D0	VOL0_L		high	low	0	R/W
0x18EB Volume Control Register	D7						
	D6						
	D5						
	D4	VOL4_R	Right volume control value (0~31)	high	low	0	R/W
	D3	VOL3_R		high	low	0	R/W
	D2	VOL2_R		high	low	0	R/W
	D1	VOL1_R		high	low	0	R/W
	D0	VOL0_R		high	low	0	R/W

11111 : 0db ; 11110 : -1.94db ; 11101 : -3.52db ; 11100 : -4.86db ; 11011 : -6.02db ;
11010 : -7.04db ; 11001 : -7.86db ; 11000 : -8.79db ; 10111 : -10.16db ; 10110 : -10.81db ;
10101 : -11.42db ; 10100 : -11.98db ; 10011 : -12.51db ; 10010 : -13.01db ;
10001 : -13.84db ; 10000 : -13.93db ; 01111 : -14.70db ; 01110 : -15.11db ;
01101 : -15.48db ; 01100 : -15.84db ; 01011 : -16.18db ; 01010 : -16.51db ;
01001 : -16.83db ; 01000 : -17.14db ; 00111 : -17.70db ; 00110 : -17.97db ;
00101 : -18.24db ; 00100 : -18.50db ; 00011 : -18.76db ; 00010 : -19.00db ;
00001 : -19.24db ; 00000 : -20.35db

CODEC control registers

Address	Bit	Name	Function	1	0	SR	R/W
0x18F0 CODEC	D7	MP3DEC_SR	MP3 decoder reset	Reset	None	0	R/W
	D6	PCMDBL	PCM double sample rate	Enable	Disable	0	R/W
	D5	RSTBP	Reset R/W Buffer Pointer	Reset	None		W
	D4	MODE3	CODEC mode select	0000 : MP3 0001 : ADPCM Decoder 0010 : ADPCM Encoder 0011 : PCM		0000	R/W
	D3	MODE2					
	D2	MODE1					
	D1	MODE0					
	D0	ENCODE TRG	Encode trigger	Trigger	None	0	R/W
0x18F1 CODEC	D7	WBFD7	Write Buffer (High Byte)	High	Low	0	R/W
	D6	WBFD6		High	Low	0	R/W
	D5	WBFD5		High	Low	0	R/W
	D4	WBFD4		High	Low	0	R/W
	D3	WBFD3		High	Low	0	R/W
	D2	WBFD2		High	Low	0	R/W
	D1	WBFD1		High	Low	0	R/W
	D0	WBFD0		High	Low	0	R/W
0x18F2 CODEC	D7	WBFD15	Write Buffer (Low Byte)	High	Low	0	R/W
	D6	WBFD14		High	Low	0	R/W
	D5	WBFD13		High	Low	0	R/W
	D4	WBFD12		High	Low	0	R/W
	D3	WBFD11		High	Low	0	R/W
	D2	WBFD10		High	Low	0	R/W
	D1	WBFD9		High	Low	0	R/W
	D0	WBFD8		High	Low	0	R/W
0x18F3 CODEC	D7	RBFD7	Read Buffer	High	Low	0	R/W
	D6	RBFD6		High	Low	0	R/W
	D5	RBFD5		High	Low	0	R/W
	D4	RBFD4		High	Low	0	R/W
	D3	RBFD3		High	Low	0	R/W
	D2	RBFD2		High	Low	0	R/W
	D1	RBFD1		High	Low	0	R/W
	D0	RBFD0		High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x18F4 CODEC	D7	BLKINT	ADPCM block finish flag	R Yes W Reset	R No W None	0	R/W
	D6	BUFWINT	CODEC buffer block write finish flag	R Yes W Reset	R No W None	0	R/W
	D5	BUFRINT	CODEC buffer block read finish flag	R Yes W Reset	R No W None	0	R/W
	D4	BUFRDY	CODEC buffer ready flag	Ready	Not Ready	1	R
	D3	EIBLK	ADPCM block finish interrupt mask register	enable	mask	0	R/W
	D2	EIBUFW	CODEC buffer block write finish interrupt mask register	enable	mask	0	R/W
	D1	EIBUFR	CODEC buffer block read finish interrupt mask register	enable	mask	0	R/W
	D0	ENREADY	Enable CODEC buffer ready signal	enable	disable	0	R/W
0x18F5 CODEC	D7	BLK1	Set Block A,B length Block Length = 2^(BKL+6) BKL = 0~3 (maximum 512 bytes)	High	Low	0	R/W
	D6	BLK0		High	Low	0	R/W
	D5	VOL5	**CODEC Volume level select** **(22db, 21.5db, 21db, 20db, 19.5db, 18.8db, 18db, 17db, 16.6db, 16db, 15db, 14.5db, 14db, 13db, 12db, 11.6db, 11db, 10db, 9.4db, 8.7db, 8db, 7db, 6.5db, 6db, 5db, 4db, 3.6db, 3db, 2db, 1.4db, 0.7db, 0db, -1.4db, -3db, -4db, -5.5db, -7db, -8db, -9.6db, -11db, -12db, -14db, -15db, -16db, -18db, -19db, -21db, -22db, -23db, -25db, -26db, -28db, -29db, -30db, -32db, -33db, -34db, -36db, -37db, -39db, -40db, -41db, -42db, -44db)**	High	Low	0	R/W
	D4	VOL4		High	Low	0	R/W
	D3	VOL3		High	Low	0	R/W
	D2	VOL2		High	Low	0	R/W
	D1	VOL1		High	Low	0	R/W
	D0	VOL0		High	Low	0	R/W
0x18F6 CODEC	D7	STEREO	Enable stereo mode	Stereo	Mono	0	R/W
	D6	TRGEQ	Trigger CODEC to using new band equalizer value	New	Old		W
	D5	B60HZ5	CODEC 60Hz band equalizer coefficients	High	Low	0	R/W
	D4	B60HZ4		High	Low	0	R/W
	D3	B60HZ3		High	Low	0	R/W
	D2	B60HZ2		High	Low	0	R/W
	D1	B60HZ1		High	Low	0	R/W
	D0	B60HZ0		High	Low	0	R/W
0x18F7 CODEC	D7	PCMBFOV	PCM buffer overrun flag	R Yes W Reset	R No W None	0	R/W
	D6	MP3BFOV	MP3 buffer overrun flag	R Yes W Reset	R No W None	0	R/W
	D5	B170HZ5	CODEC 170Hz band equalizer coefficients	High	Low	0	R/W
	D4	B170HZ4		High	Low	0	R/W
	D3	B170HZ3		High	Low	0	R/W
	D2	B170HZ2		High	Low	0	R/W
	D1	B170HZ1		High	Low	0	R/W
	D0	B170HZ0		High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x18F8 CODEC	D7	PCMFULL	PCM FIFO full	Full	No full	0	R
	D6	PCM EMPTY	PCM FIFO empty	Empty	No empty	1	R
	D5	B310HZ5	CODEC 310Hz band equalizer coefficients	High	Low	0	R/W
	D4	B310HZ4		High	Low	0	R/W
	D3	B310HZ3		High	Low	0	R/W
	D2	B310HZ2		High	Low	0	R/W
	D1	B310HZ1		High	Low	0	R/W
	D0	B310HZ0		High	Low	0	R/W
0x18F9 CODEC	D7	MP3FULL	MP3 FIFO full	Full	No full	0	R
	D6	MP3 EMPTY	MP3 FIFO empty	Empty	No empty	1	R
	D5	B600HZ5	CODEC 600Hz band equalizer coefficients	High	Low	0	R/W
	D4	B600HZ4		High	Low	0	R/W
	D3	B600HZ3		High	Low	0	R/W
	D2	B600HZ2		High	Low	0	R/W
	D1	B600HZ1		High	Low	0	R/W
	D0	B600HZ0		High	Low	0	R/W
0x18FA CODEC	D7						
	D6						
	D5	B1KHZ5	CODEC 1KHz band equalizer coefficients	High	Low	0	R/W
	D4	B1KHZ4		High	Low	0	R/W
	D3	B1KHZ3		High	Low	0	R/W
	D2	B1KHZ2		High	Low	0	R/W
	D1	B1KHZ1		High	Low	0	R/W
	D0	B1KHZ0		High	Low	0	R/W
0x18FB CODEC	D7						
	D6						
	D5	B3KHZ5	CODEC 3KHz band equalizer coefficients	High	Low	0	R/W
	D4	B3KHZ4		High	Low	0	R/W
	D3	B3KHZ3		High	Low	0	R/W
	D2	B3KHZ2		High	Low	0	R/W
	D1	B3KHZ1		High	Low	0	R/W
	D0	B3KHZ0		High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x18FC CODEC	D7						
	D6						
	D5	B6KHZ5	CODEC 6KHz band equalizer coefficients	High	Low	0	R/W
	D4	B6KHZ4		High	Low	0	R/W
	D3	B6KHZ3		High	Low	0	R/W
	D2	B6KHZ2		High	Low	0	R/W
	D1	B6KHZ1		High	Low	0	R/W
	D0	B6KHZ0		High	Low	0	R/W
0x18FD CODEC	D7						
	D6						
	D5	B12KHZ5	CODEC 12KHz band equalizer coefficients	High	Low	0	R/W
	D4	B12KHZ4		High	Low	0	R/W
	D3	B12KHZ3		High	Low	0	R/W
	D2	B12KHZ2		High	Low	0	R/W
	D1	B12KHZ1		High	Low	0	R/W
	D0	B12KHZ0		High	Low	0	R/W
0x18FE CODEC	D7						
	D6						
	D5	B14KHZ5	CODEC 14KHz band equalizer coefficients	High	Low	0	R/W
	D4	B14KHZ4		High	Low	0	R/W
	D3	B14KHZ3		High	Low	0	R/W
	D2	B14KHZ2		High	Low	0	R/W
	D1	B14KHZ1		High	Low	0	R/W
	D0	B14KHZ0		High	Low	0	R/W
0x18FF CODEC	D7						
	D6						
	D5	B16KHZ5	CODEC 16KHz band equalizer coefficients	High	Low	0	R/W
	D4	B16KHZ4		High	Low	0	R/W
	D3	B16KHZ3		High	Low	0	R/W
	D2	B16KHZ2		High	Low	0	R/W
	D1	B16KHZ1		High	Low	0	R/W
	D0	B16KHZ0		High	Low	0	R/W

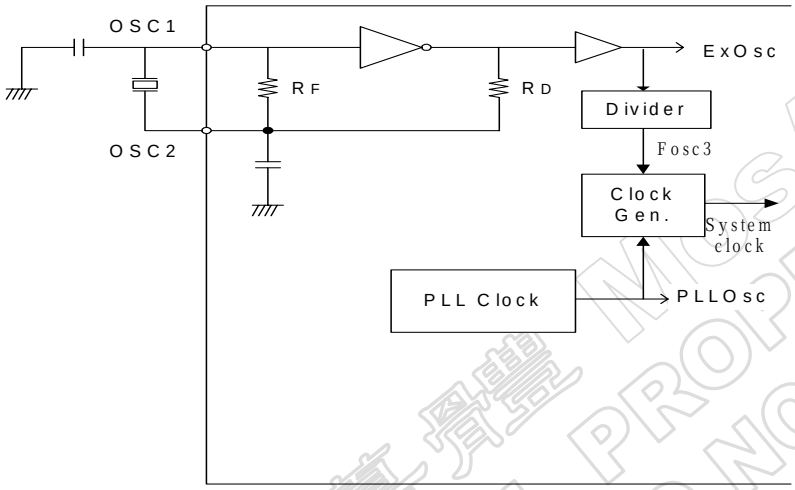
UART control registers

Address	Bit	Name	Function	1	0	SR	R/W
0x1834 UART	D7	TBRD7	Transmit/Received Buffer Registers TBR[7:0]	High	Low	0	R/W
	D6	TBRD6		High	Low	0	R/W
	D5	TBRD5		High	Low	0	R/W
	D4	TBRD4		High	Low	0	R/W
	D3	TBRD3		High	Low	0	R/W
	D2	TBRD2		High	Low	0	R/W
	D1	TBRD1		High	Low	0	R/W
	D0	TBRD0		High	Low	0	R/W
0x1835 UART	D7	SM00	Operating Mode	00 : 8 bit UART (CpuClk/12) 01 : 8 bit UART (Variable Rate) 10: 9 bit UART (CpuClk/16) 11 : 9 bit UART (Variable Rate)		01	R/W
	D6	SM01					
	D5						
	D4	REN	Enable Receive data (this bit will be clear to 0 after receive interrupt)	Enable Trigger	Disable	0	R/W
	D3	TB08	The 9th transmitted data bit	High	Low	0	R/W
	D2	RB08	The 9th received data bit	High	Low	0	R
	D1	TXINT	Transmit interrupt flag	R Yes W Reset	R No W None	0	R/W
	D0	RXINT	Receive interrupt flag	R Yes W Reset	R No W None	0	R/W
0x1836 UART	D7						
	D6						
	D5						
	D4						
	D3						
	D2						
	D1	ENTXINT	Enable Transmit Interrupt	Enable	Disable	0	R/W
	D0	ENRXINT	Enable Receive Interrupt	Enable	Disable	0	R/W
0x1837 UART	D7	UPreDIV7	UART clock pre-divider UART clock = CpuClk / (UPreDIV+1)*(UPostDIV+1)	high	low	0	R/W
	D6	UPreDIV6		high	low	0	R/W
	D5	UPreDIV5		high	low	0	R/W
	D4	UPreDIV4		high	low	0	R/W
	D3	UPreDIV3		high	low	0	R/W
	D2	UPreDIV2		high	low	0	R/W
	D1	UPreDIV1		high	low	0	R/W
	D0	UPreDIV0		high	low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x1838 UART	D7	UPostDIV7	UART clock post-divider UART clock = CpuClk / (UPreDIV+1)*(UPostDIV+1)	high	low	0	R/W
	D6	UPostDIV6		high	low	0	R/W
	D5	UPostDIV5		high	low	0	R/W
	D4	UPostDIV4		high	low	0	R/W
	D3	UPostDIV3		high	low	0	R/W
	D2	UPostDIV2		high	low	0	R/W
	D1	UPostDIV1		high	low	0	R/W
	D0	UPostDIV0		high	low	0	R/W

5.2 CLOCK GENERATOR & PHASE LOCKED LOOP

MA8201-H72 has a built-in RC oscillator for the purpose of power saving. The frequency is about 32KHz. User can easily change the CPU system clock between 32KHz, divided PLL clock, divided external 48MHz clock. User also can use the pre-scale registers SCLK2, SCLK1, SCLK0 to change the system clock. The application circuit is as follow :



Address	Bit	Name	Function	1	0	SR	R/W
0x1800 SYS Control	D7	CLKCHG1	CPU(system) operating clock switch	00 : 32KHz 01 : 48MHz	10 : PLLCLK 11 : 48MHz	00	R/W
	D6	CLKCHG0					
	D5						
	D4	RCON	RC oscillator On/Off	On	Off	1	R/W
	D3	SCLK2	System clock for high speed clock select (EXCLK or PLLCLK)	000 : ExOsc 001 : ExOsc/2 010 : ExOsc/3 011 : ExOsc/4	100 : ExOsc/5 101 : ExOsc/6 110 : ExOsc/7 111 : ExOsc/8	001	R/W
	D2	SCLK1					
	D1	SCLK0					
	D0	EXCLKON	External Oscillator(48MHz) On/Off	On	Off	0	R/W

D7-D6 : CPU(system) operating clock select, 00 = 32KHz, 01 = 48MHz, 10 = PLL clock, 11 = 48MHz

D4 : RC Oscillator On/Off, 1 = On, 0 = Off

D[3:1] : Fosc3 Clock select, 0 = ExOsc, 1 = ExOsc/2, 2 = ExOsc/3, 3 = ExOsc/4, 4 = ExOsc/5, 5 = ExOsc/6, 6 = ExOsc/7, 7 = ExOsc/8

D0 : External Oscillator (48MHz) On/Off, 1 = On, 0 = Off

Address	Bit	Name	Function	1	0	SR	R/W
0x1801 SYS Control	D7	USBSUS	USB suspend request	Request	No request	0	R
	D6	PCSTBY	PC standby request	Request	No request	0	R
	D5	FWR2SUS	System ready to suspend	R Suspend W Ready	R Normal W none	0	R/W
	D4	SusThrd 2	The PC standby status detect threshold	T= 32* (SusThrd[2:0] +1) ms T=32ms – 256ms		1	R/W
	D3	SusThrd 1				1	R/W
	D2	SusThrd 0				1	R/W
	D1	WS1	Wait state	00 : 0 wait state 01 : 1 wait state 10 :2 wait state 11 : 3 wait state		00	R/W
	D0	WS0					

D7 : USB suspend request. 0: the system detect the suspend request.

1: there are no suspend request from host.

D6 : PC standby request. 0: The system detect the PC enter the standby mode.

1: The system work normally

D5 : F/W ready to suspend. Write1 : if the CPU clock change to ROSC and turn off the fosc3, the system will enter the suspend mode.

Write0 : no operate

Read 1: During suspend state

Read 0: system not at suspend state

D4 ~ D2 : The PC standby status detect threshold

The Threshold = 32 * (SusThrd[2:0] +1) ms

D1 ~ D0 : CPU wait state. 00 : 0 wait state 01 : 1 wait state 10 :2 wait state 11 : 3 wait state

Address	Bit	Name	Function	1	0	SR	R/W
0x1802 SYS Control	D7						
	D6						
	D5	MPU_ST	CPU status	MPU	Normal	0	R
	D4	BUP	CLKIN oscillator speed up register	On	Off	1	R/W
	D3						
	D2						
	D1						
	D0	WDEN	Watchdog enable	enable	disable	0	R/W

D5 : CPU mode select, 0 : Normal, 1: MPU mode

D4 : CLKIN oscillator (10MHz) speed up, 0 : no speed up, 1 : speed up

D0 : Watchdog enable. 1 : enable, 0 : disable.

Address	Bit	Name	Function	1		0		SR	R/W
0x1809 PLL	D7								
	D6								
	D5	IPLL	PLL interrupt factor flag	R W	Yes Reset	R W	No None	0	R/W
	D4	EIPLL	PLL interrupt mask register	Enable		Mask		0	R/W
	D3								
	D2	FpllCHG	Frequency change trigger register	Change		No change		0	W
	D1	PLLON	Turn on phase locked loop	Yes		No		0	R/W
	D0	DN8						0	W
0x180A PLL	D7	DN7	Phase locked loop (PLL) divide factor (DN8-DN0=5-512)	The PLL output : Fpll = divide factor * 32KHz				10H	R/W
	D6	DN6							
	D5	DN5							
	D4	DN4							
	D3	DN3							
	D2	DN2							
	D1	DN1							
	D0	DN0							

D5 : PLL interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D4 : PLL interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

D2 : Frequency change trigger register, 1 = change, 0 = no change

D1 : turn on/off PLL function, 0 = off, 1 = on

D0 : PLL divider factor, Fpll = divider factor (DN8 - DN0 + 1) * 32KHz

The phase locked loop can generate a high frequency to the CPU and peripheral. The frequency can be calculate by the formula Fpll = divider factor * 32KHz. The divider factor is equal to the number of data DN8-DN0 plus 1. The range of divider factor is about 5-512. The application circuit needs an external capacitor as low pass filter. When turn on the PLL, it will generator an interrupt to the CPU at the stability of PLL. User can easily change the CPU system clock after receiving the interrupt. When the PLL operates, user can change the PLL frequency output by setting the register FpllCHG, but it need few mini-second to be stable. The system will stop during these time. User must avoid to using peripherals depending on the frequency of PLL.

Address	Bit	Name	Function	1	0	SR	R/W
0x180B PLL	D7	DLY7	Phase locked loop (PLL) ready time (4ms*(DLY+1))	High	Low	0CH	R/W
	D6	DLY6		High	Low		
	D5	DLY5		High	Low		
	D4	DLY4		High	Low		
	D3	DLY3		High	Low		
	D2	DLY2		High	Low		
	D1	DLY1		High	Low		
	D0	DLY0		High	Low		

D[7:0] : PLL ready time, PLL ready time = 4ms*(DLY+1)

5.3 WATCHDOG TIMER (WDT)

The watchdog timer is used to resume or restart the core processor of MA8201-H72 when it is disturbed by malfunctions such as noise, power surge and system out of control. When watchdog timer times out, it will generate a reset pulse with duration of minimum 250 ms.

Address	Bit	Name	Function	1	0	SR	R/W
0x1803 Watchdog Timer	D7	WDTRST	Reset watchdog timer	Reset	Normal	0	R/W
	D6	WDTP6	Watchdog time selection (1-128 sec.)	The watchdog time = 1-128 sec.		10H (17 sec)	R/W
	D5	WDTP5					
	D4	WDTP4					
	D3	WDTP3					
	D2	WDTP2					
	D1	WDTP1					
	D0	WDTP0					

D7 : reset watchdog timer, 0 = normal, 1 = reset

D[6:0] : watchdog timer select, 1-128 seconds

5.4 Port Function Selection Function Control Registers

Address	Bit	Name	Function	1	0	SR	R/W
0x1804 Port Function selection	D7	SPISEL1	P31-P33 I/O Port function selection	00 : Normal 01 : IIS	10 : SPI 11 : SPI	00	R/W
	D6	SPISEL0					
	D5	PXCE2	NAND Flash XCE pin select	000:P16 001:P17 010:P21 011:P22	100:P23 101:P24 100:P30 101:P31	0	R/W
	D4	PXCE1					
	D3	PXCE0					
	D2	PFSEL2	I/O Port function selection	100 : Port assign as NAND FLASH I/O 101 : Port assign as SD card I/O others : Normal I/O port		0	R/W
	D1	PFSEL1					
	D0	PFSEL0					

D7~ D6 : P31-P33 I/O Port function selection, 00 : Normal, 01 : IIS, 10 & 11 : SPI

D5 ~ D3 : NAND Flash XCE pin select. See the definition above.

D2 ~ D0 : I/O Port function selection. See the definition above.

Address	Bit	Name	Function	1	0	SR	R/W
0x1805 Low power Control	D7	LPWDMA	DMA controller system clock stop	Stop	Normal	0	R/W
	D6	LPWUSB	USB controller system clock stop	Stop	Normal	0	R/W
	D5	LPWCTM	CTM controller system clock stop	Stop	Normal	0	R/W
	D4	LPWPTM	PTM controller system clock stop	Stop	Normal	0	R/W
	D3	LPWSPI	SPI controller system clock stop	Stop	Normal	0	R/W
	D2	LPWSM	NAND FLASH controller system clock stop	Stop	Normal	0	R/W
	D1	LPWSD	SD controller system clock stop	stop	Normal	0	R/W
	D0	LPWCODEC	CODEC decode system clock stop	stop	Normal	0	R/W

D7 : DMA controller system clock stop, 1 : stop, 0 : normal

D6 : USB controller system clock stop, 1 : stop, 0 : normal

D5 : CTM controller system clock stop, 1 : stop, 0 : normal

D4 : PTM controller system clock stop, 1 : stop, 0 : normal

D3 : SPI controller system clock stop, 1 : stop, 0 : normal

D2 : NAND FLASH controller system clock stop, 1 : stop, 0 : normal

D1 : SD controller system clock stop, 1 : stop, 0 : normal

D0 : CODEC decode clock stop, 1 : stop, 0 : normal

Address	Bit	Name	Function	1	0	SR	R/W
0x1806 Low power Control	D7	RSTDMA	USB controller reset	reset	none	0	W
	D6	RSTUSB	USB controller reset	reset	none	0	W
	D5	RSTCTM	CTM controller reset	reset	none	0	W
	D4	RSTPTM	PTM controller reset	reset	none	0	W
	D3	RSTSPI	SPI controller reset	reset	none	0	W
	D2	RSTSM	NAND FLASH controller reset	reset	none	0	W
	D1	RSTSD	SD controller reset	reset	none	0	W
	D0	RSTCODEC	CODEC decode reset	reset	none	0	W

D7 : DMA controller reset, 1 : reset, 0 : none

D6 : USB controller reset, 1 : reset, 0 : none

D5 : CTM controller reset, 1 : reset, 0 : none

D4 : PTM controller reset, 1 : reset, 0 : none

D3 : SPI controller reset, 1 : reset, 0 : none

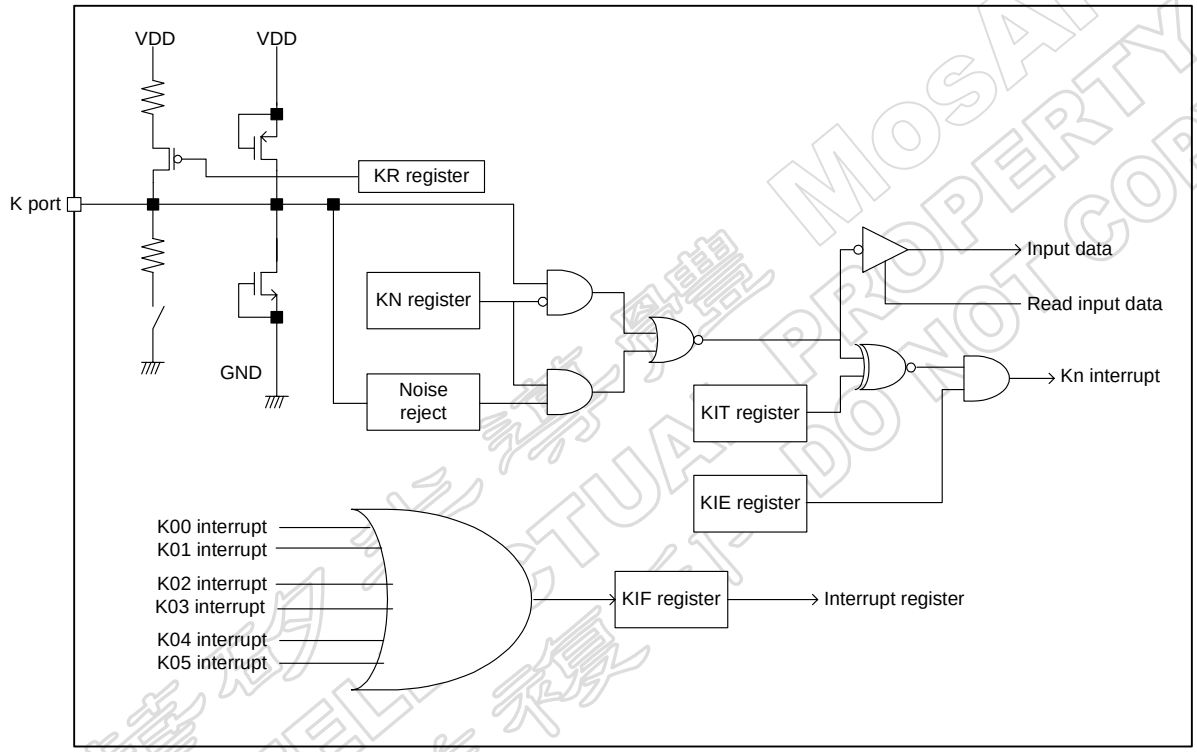
D2 : NAND FLASH controller reset, 1 : reset, 0 : none

D1 : SD controller reset, 1 : reset, 0 : none

D0 : CODEC decode reset, 1 : reset, 0 : none

5.5 INPUT PORTS

The input pins K05-K00 consist of noise reject circuits selected by the registers K05N-K00N individually. When user sets the interrupt trigger mode, the input pins will generate an interrupt to the CPU at the falling or rising edge of input signal. User can check the K05-K00 data to assure the interrupt source. Each port can be configured by software to meet various system and design requirement. There are software switches to select pull-up resistors at the K05-K00 pins. The input port function block is shown as follow :



Address	Bit	Name	Function	1	0	SR	R/W
0x1810 Input Port	D5	KIT05	Input port K05 interrupt trigger mode	Falling	Rising	1	R/W
	D4	KIT04	Input port K04 interrupt trigger mode	Falling	Rising	1	R/W
	D3	KIT03	Input port K03 interrupt trigger mode	Falling	Rising	1	R/W
	D2	KIT02	Input port K02 interrupt trigger mode	Falling	Rising	1	R/W
	D1	KIT01	Input port K01 interrupt trigger mode	Falling	Rising	1	R/W
	D0	KIT00	Input port K00 interrupt trigger mode	Falling	Rising	1	R/W

D[5:0] : input port K05-K00 interrupt trigger mode, 1 = falling, 0 = rising

Address	Bit	Name	Function	1	0	SR	R/W
0x1811 Input Port	D5	K05R	Input port K05 pull-up resister select	On	Off	1	R/W
	D4	K04R	Input port K04 pull-up resister select	On	Off	1	R/W
	D3	K03R	Input port K03 pull-up resister select	On	Off	1	R/W
	D2	K02R	Input port K02 pull-up resister select	On	Off	1	R/W
	D1	K01R	Input port K01 pull-up resister select	On	Off	1	R/W
	D0	K00R	Input port K00 pull-up resister select	On	Off	1	R/W

D[5:0] : input port K05-K00 pull-up resister on/off select, 1 = on, 0 = off

Address	Bit	Name	Function	1	0	SR	R/W
0x1812 Input Port	D5	K05N	Input port K05 noise reject select	With noise rej.	No noise rej.	0	R/W
	D4	K04N	Input port K04 noise reject select	With noise rej.	No noise rej.	0	R/W
	D3	K03N	Input port K03 noise reject select	With noise rej.	No noise rej.	0	R/W
	D2	K02N	Input port K02 noise reject select	With noise rej.	No noise rej.	0	R/W
	D1	K01N	Input port K01 noise reject select	With noise rej.	No noise rej.	0	R/W
	D0	K00N	Input port K00 noise reject select	With noise rej.	No noise rej.	0	R/W

D[5:0] : input port K05-K00 noise reject circuit select (31.25ms), 1 = with, 0 = no

Address	Bit	Name	Function	1	0	SR	R/W
0x1813 Input Port	D5	K05	Input port K05 data	High	Low		R
	D4	K04	Input port K04 data	High	Low		R
	D3	K03	Input port K03 data	High	Low		R
	D2	K02	Input port K02 data	High	Low		R
	D1	K01	Input port K01 data	High	Low		R
	D0	K00	Input port K00 data	High	Low		R

D[5:0] : input port K05-K00 data, read only

Address	Bit	Name	Function	1		0		SR	R/W
0x1814 Input Port	D0	IK0	Input port K03-K00 interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		

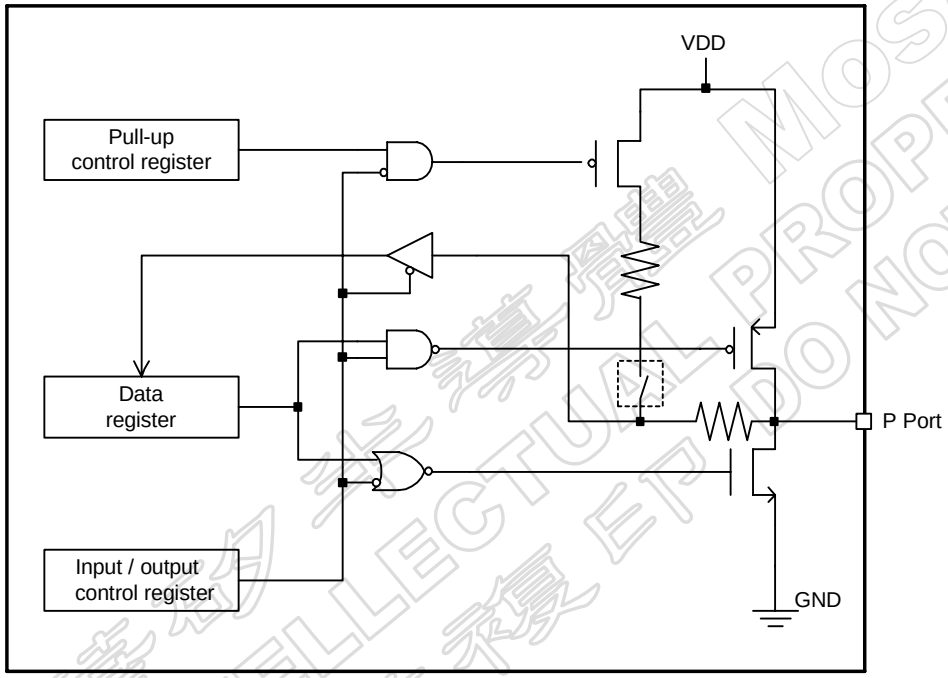
D[0] : input port K05-K00 interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

Address	Bit	Name	Function	1	0	SR	R/W
0x1815 Input Port	D5	EIK05	Input port K05 interrupt mask register	Enable	Mask	0	R/W
	D4	EIK04	Input port K04 interrupt mask register	Enable	Mask	0	R/W
	D3	EIK03	Input port K03 interrupt mask register	Enable	Mask	0	R/W
	D2	EIK02	Input port K02 interrupt mask register	Enable	Mask	0	R/W
	D1	EIK01	Input port K01 interrupt mask register	Enable	Mask	0	R/W
	D0	EIK00	Input port K00 interrupt mask register	Enable	Mask	0	R/W

D[5:0] : input port K05-K00 interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

5.6 INPUT/OUTPUT PORTS

The MA8201-H72 has four input/output ports P07-P00, P17-P10, P27-P20, P33-P30 and P47-P40. The input/output ports have different special functions. Please refer the PIN LAYOUT DIAGRAM page 6-7.Each port can be configured by software to meet various system and design requirements. User can also select the pull-up resistors at the input/output pins. Furthermore, user can select the direction of input/output pins. When user selects the special function, the input/output direction registers will be invalid. There are hardware switches to select pull-up resistors at the input/output pins. The detail description about the function as follow :



The function block of input/output port

Address	Bit	Name	Function	1	0	SR	R/W
0x1820 I/O Port	D7	P07D	Input/output port P07 direction select	Output	Input	0	R/W
	D6	P06D	Input/output port P06 direction select	Output	Input	0	R/W
	D5	P05D	Input/output port P05 direction select	Output	Input	0	R/W
	D4	P04D	Input/output port P04direction select	Output	Input	0	R/W
	D3	P03D	Input/output port P03 direction select	Output	Input	0	R/W
	D2	P02D	Input/output port P02 direction select	Output	Input	0	R/W
	D1	P01D	Input/output port P01 direction select	Output	Input	0	R/W
	D0	P00D	Input/output port P00 direction select	Output	Input	0	R/W
0x1823 I/O Port	D7	P17D	Input/output port P17 direction select	Output	Input	0	R/W
	D6	P16D	Input/output port P16 direction select	Output	Input	0	R/W
	D5	P15D	Input/output port P15 direction select	Output	Input	0	R/W
	D4	P14D	Input/output port P14 direction select	Output	Input	0	R/W
	D3	P13D	Input/output port P13 direction select	Output	Input	0	R/W
	D2	P12D	Input/output port P12 direction select	Output	Input	0	R/W
	D1	P11D	Input/output port P11 direction select	Output	Input	0	R/W
	D0	P10D	Input/output port P10 direction select	Output	Input	0	R/W
0x1826 I/O Port	D7	P27D	Input/output port P27 direction select	Output	Input	0	R/W
	D6	P26D	Input/output port P26 direction select	Output	Input	0	R/W
	D5	P25D	Input/output port P25 direction select	Output	Input	0	R/W
	D4	P24D	Input/output port P24 direction select	Output	Input	0	R/W
	D3	P23D	Input/output port P23 direction select	Output	Input	0	R/W
	D2	P22D	Input/output port P22 direction select	Output	Input	0	R/W
	D1	P21D	Input/output port P21 direction select	Output	Input	0	R/W
	D0	P20D	Input/output port P20 direction select	Output	Input	0	R/W
0x1829 I/O Port	D3	P33D	Input/output port P33 direction select	Output	Input	0	R/W
	D2	P32D	Input/output port P32 direction select	Output	Input	0	R/W
	D1	P31D	Input/output port P31 direction select	Output	Input	0	R/W
	D0	P30D	Input/output port P30 direction select	Output	Input	0	R/W
0x182C I/O Port	D7	P47D	Input/output port P47 direction select	Output	Input	0	R/W
	D6	P46D	Input/output port P46 direction select	Output	Input	0	R/W
	D5	P45D	Input/output port P45 direction select	Output	Input	0	R/W
	D4	P44D	Input/output port P44direction select	Output	Input	0	R/W
	D3	P43D	Input/output port P43 direction select	Output	Input	0	R/W
	D2	P42D	Input/output port P42 direction select	Output	Input	0	R/W
	D1	P41D	Input/output port P41 direction select	Output	Input	0	R/W
	D0	P40D	Input/output port P40 direction select	Output	Input	0	R/W

D[7:0] : input/output port direction select, 0 = input, 1 = output

Address	Bit	Name	Function	1	0	SR	R/W
0x1821 I/O Port	D7	P07R	P07 pull-up resister select	On	Off	1	R/W
	D6	P06R	P06 pull-up resister select	On	Off	1	R/W
	D5	P05R	P05 pull-up resister select	On	Off	1	R/W
	D4	P04R	P04 pull-up resister select	On	Off	1	R/W
	D3	P03R	P03 pull-up resister select	On	Off	1	R/W
	D2	P02R	P02 pull-up resister select	On	Off	1	R/W
	D1	P01R	P01 pull-up resister select	On	Off	1	R/W
	D0	P00R	P00 pull-up resister select	On	Off	1	R/W
0x1824 I/O Port	D7	P17R	P17 pull-up resister select	On	Off	1	R/W
	D6	P16R	P16 pull-up resister select	On	Off	1	R/W
	D5	P15R	P15 pull-up resister select	On	Off	1	R/W
	D4	P14R	P14 pull-up resister select	On	Off	1	R/W
	D3	P13R	P13 pull-up resister select	On	Off	1	R/W
	D2	P12R	P12 pull-up resister select	On	Off	1	R/W
	D1	P11R	P11 pull-up resister select	On	Off	1	R/W
	D0	P10R	P10 pull-up resister select	On	Off	1	R/W
0x1827 I/O Port	D7	P27R	P27 pull-up resister select	On	Off	1	R/W
	D6	P26R	P26 pull-up resister select	On	Off	1	R/W
	D5	P25R	P25 pull-up resister select	On	Off	1	R/W
	D4	P24R	P24 pull-up resister select	On	Off	1	R/W
	D3	P23R	P23 pull-up resister select	On	Off	1	R/W
	D2	P22R	P22 pull-up resister select	On	Off	1	R/W
	D1	P21R	P21 pull-up resister select	On	Off	1	R/W
	D0	P20R	P20 pull-up resister select	On	Off	1	R/W
0x182A I/O Port	D3	P33R	P33 pull-up resister select	On	Off	1	R/W
	D2	P32R	P32 pull-up resister select	On	Off	1	R/W
	D1	P31R	P31 pull-up resister select	On	Off	1	R/W
	D0	P30R	P30 pull-up resister select	On	Off	1	R/W
0x182D I/O Port	D7	P47R	P47 pull-up resister select	On	Off	1	R/W
	D6	P46R	P46 pull-up resister select	On	Off	1	R/W
	D5	P45R	P45 pull-up resister select	On	Off	1	R/W
	D4	P44R	P44 pull-up resister select	On	Off	1	R/W
	D3	P43R	P43 pull-up resister select	On	Off	1	R/W
	D2	P42R	P42 pull-up resister select	On	Off	1	R/W
	D1	P41R	P41 pull-up resister select	On	Off	1	R/W
	D0	P40R	P40 pull-up resister select	On	Off	1	R/W

D[7:0] : input/output port pull-up resistor select, 1 = with, 0 = without

Address	Bit	Name	Function	1	0	SR	R/W
0x1822 I/O Port	D7	P07	Input/output port P07 data	High	Low	1	R/W
	D6	P06	Input/output port P06 data	High	Low	1	R/W
	D5	P05	Input/output port P05 data	High	Low	1	R/W
	D4	P04	Input/output port P04 data	High	Low	1	R/W
	D3	P03	Input/output port P03 data	High	Low	1	R/W
	D2	P02	Input/output port P02 data	High	Low	1	R/W
	D1	P01	Input/output port P01 data	High	Low	1	R/W
	D0	P00	Input/output port P00 data	High	Low	1	R/W
0x1825 I/O Port	D7	P17	Input/output port P17 data	High	Low	1	R/W
	D6	P16	Input/output port P16 data	High	Low	1	R/W
	D5	P15	Input/output port P15 data	High	Low	1	R/W
	D4	P14	Input/output port P14 data	High	Low	1	R/W
	D3	P13	Input/output port P13 data	High	Low	1	R/W
	D2	P12	Input/output port P12 data	High	Low	1	R/W
	D1	P11	Input/output port P11 data	High	Low	1	R/W
	D0	P10	Input/output port P10 data	High	Low	1	R/W
0x1828 I/O Port	D7	P27	Input/output port P27 data	High	Low	1	R/W
	D6	P26	Input/output port P26 data	High	Low	1	R/W
	D5	P25	Input/output port P25 data	High	Low	1	R/W
	D4	P24	Input/output port P24 data	High	Low	1	R/W
	D3	P23	Input/output port P23 data	High	Low	1	R/W
	D2	P22	Input/output port P22 data	High	Low	1	R/W
	D1	P21	Input/output port P21 data	High	Low	1	R/W
	D0	P20	Input/output port P20 data	High	Low	1	R/W
0x182B I/O Port	D3	P33	Input/output port P33 data	High	Low	1	R/W
	D2	P32	Input/output port P32 data	High	Low	1	R/W
	D1	P31	Input/output port P31 data	High	Low	1	R/W
	D0	P30	Input/output port P30 data	High	Low	1	R/W
0x182E I/O Port	D7	P47	Input/output port P47 data	High	Low	1	R/W
	D6	P46	Input/output port P46 data	High	Low	1	R/W
	D5	P45	Input/output port P45 data	High	Low	1	R/W
	D4	P44	Input/output port P44 data	High	Low	1	R/W
	D3	P43	Input/output port P43 data	High	Low	1	R/W
	D2	P42	Input/output port P42 data	High	Low	1	R/W
	D1	P41	Input/output port P41 data	High	Low	1	R/W
	D0	P40	Input/output port P40 data	High	Low	1	R/W

D[7:0] : input/output data

The directions of PPORT will be forced to input or output by hardware in some special functions :

P10, P11, P14, P15, P16, P17 are output in Nand Flash mode(1804, D2=1, D1=0, D0=0)

P30 is always output

P31, P32 are output in Nand Flash mode(1804, D2=1, D1=0, D0=0) or in SPI mode(1804, D7=1, D6=0) or in IIS mode(1804, D7=0, D6=1)

P33 are output in IIS mode(1804, D7=0, D6=1)

5.7 CLOCK TIMER

The clock timer interrupt is generated at the falling edge of the frequencies (64Hz, 32Hz, 16Hz, 8Hz, 4Hz, 2Hz, 1Hz). At this time, the corresponding interrupt factor flag (IC64, ICT32, ICT16, ICT8, ICT4, ICT2, ICT1) is set to 1.

Selection of masking which separate interrupts can be made with the interrupt mask registers (ECT64, ECT32, ECT16, ECT8, ECT4, ECT2, ECT1). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to 1 at the falling edge of the corresponding signal.

Address	Bit	Name	Function	1	0	SR	R/W
0x1830	D1	CTRST	Clock timer reset	Reset	No operation		W
Clock Timer	D0	CTRUN	Clock timer run/stop control	Run	Stop	0	R/W

D0 : reset clock timer, write only, 1 = reset , 0 = no operation

D1 : clock timer run/stop control, 1 = run , 0 = stop

Address	Bit	Name	Function	1	0	SR	R/W
0x1831 Clock Timer	D7	CT1D	Clock timer data 1 Hz	High	Low	0	R
	D6	CT2D	Clock timer data 2 Hz	High	Low	0	R
	D5	CT4D	Clock timer data 4 Hz	High	Low	0	R
	D4	CT8D	Clock timer data 8 Hz	High	Low	0	R
	D3	CT16D	Clock timer data 16 Hz	High	Low	0	R
	D2	CT32D	Clock timer data 32 Hz	High	Low	0	R
	D1	CT64D	Clock timer data 64 Hz	High	Low	0	R
	D0	CT128D	Clock timer data 128 Hz	High	Low	0	R

D[7:0] : clock timer data

Address	Bit	Name	Function	1		0		SR	R/W
0x1832 Clock Timer	D6	ICT64	Clock timer 64 Hz interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D5	ICT32	Clock timer 32 Hz interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D4	ICT16	Clock timer 16 Hz interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D3	ICT8	Clock timer 8 Hz interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D2	ICT4	Clock timer 4 Hz interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D1	ICT2	Clock timer 2 Hz interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D0	ICT1	Clock timer 1 Hz interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		

D6 : clock timer 64 Hz interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D5 : clock timer 32 Hz interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D4 : clock timer 16 Hz interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D3 : clock timer 8 Hz interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D2 : clock timer 4 Hz interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D1 : clock timer 2 Hz interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D0 : clock timer 1 Hz interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

Address	Bit	Name	Function	1	0	SR	R/W
0x1833 Clock Timer	D6	ECT64	Clock timer 64 Hz interrupt mask register	Enable	Mask	0	R/W
	D5	ECT32	Clock timer 32 Hz interrupt mask register	Enable	Mask	0	R/W
	D4	ECT16	Clock timer 16 Hz interrupt mask register	Enable	Mask	0	R/W
	D3	ECT8	Clock timer 8 Hz interrupt mask register	Enable	Mask	0	R/W
	D2	ECT4	Clock timer 4 Hz interrupt mask register	Enable	Mask	0	R/W
	D1	ECT2	Clock timer 2 Hz interrupt mask register	Enable	Mask	0	R/W
	D0	ECT1	Clock timer 1 Hz interrupt mask register	Enable	Mask	0	R/W

D6 : clock timer 64 Hz interrupt mask register, 0 = disable interrupt, 1 = enable interrupt

D5 : clock timer 32 Hz interrupt mask register, 0 = disable interrupt, 1 = enable interrupt

D4 : clock timer 16 Hz interrupt mask register, 0 = disable interrupt, 1 = enable interrupt

D3 : clock timer 8 Hz interrupt mask register, 0 = disable interrupt, 1 = enable interrupt

D2 : clock timer 4 Hz interrupt mask register, 0 = disable interrupt, 1 = enable interrupt

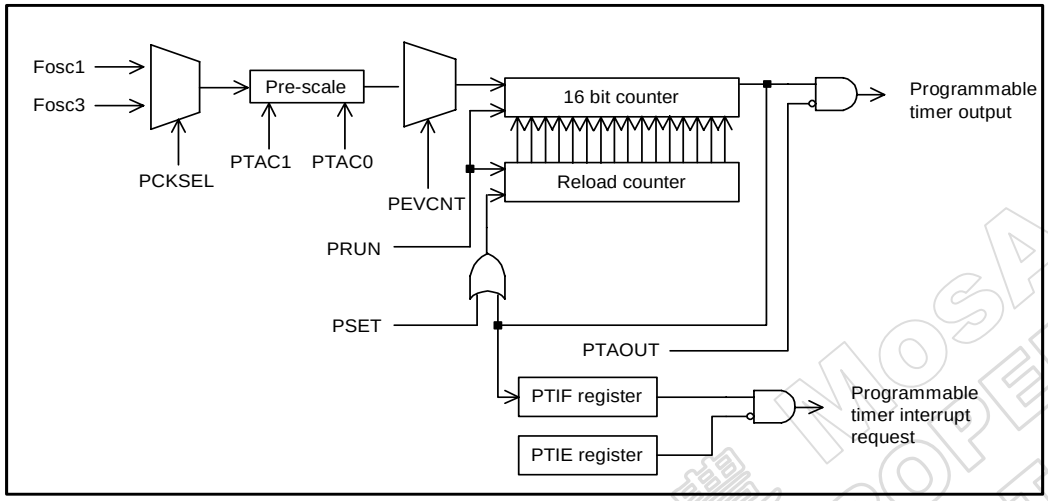
D1 : clock timer 2 Hz interrupt mask register, 0 = disable interrupt, 1 = enable interrupt

D0 : clock timer 1 Hz interrupt mask register, 0 = disable interrupt, 1 = enable interrupt

5.8 16-BIT PROGRAMMBLE TIMER 0/1

The MA8201-H72 has two programmable timers 0 and 1.

The programmable timer function block is as follow :



Address	Bit	Name	Function	1		0		SR	R/W
0x1840	D1	IP0	Timer0 interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
Prog. Timer0	D0	EIP0	Timer0 interrupt mask register	Enable		Mask		0	R/W

D0 : programmable timer 0 interrupt mask register, 0 = disable interrupt, 1 = enable interrupt

D1 : programmable timer 0 interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

Address	Bit	Name	Function	1	0	SR	R/W
0x1841 Prog. Timer0	D6	P0SET	Timer0 preset	Preset	None	0	W
	D5	P0RUN	Timer0 run/stop control	Run	Stop	0	R/W
	D4						
	D3	P0CONT	Timer0 continuous/one shot select	Continuous	One shot	0	R/W
	D2	P0CKSEL	Programmable timer0 clock source	Fosc3	32KHz	0	R/W
	D1	P0SC1	Programmable timer0 pre-scale clock source selection	00 : clock/1 01 : clock/4	10 : clock/16 11: clock/64	00	R/W
	D0	P0SC0					

D6 : preset data to programmable timer, 0 = none, 1 = preset, write only

D5 : turn on programmable timer, 0 = stop, 1 = run

D3 : programmable timer output type, 0 = one shot, 1 = continuous

D2 : programmable timer clock source, 0 = 32KHz, 1 = Fosc3

D[1:0] : programmable timer pre-scale clock source, 0 = clock, 1 = clock/4, 2 = clock/16, 3 = clock/64

Address	Bit	Name	Function	1	0	SR	R/W
0x1842 Prog. Timer0	D7	P0RLD7	Timer0 reload data D7	High	Low	0	R/W
	D6	P0RLD6	Timer0 reload data D6	High	Low	0	R/W
	D5	P0RLD5	Timer0 reload data D5	High	Low	0	R/W
	D4	P0RLD4	Timer0 reload data D4	High	Low	0	R/W
	D3	P0RLD3	Timer0 reload data D3	High	Low	0	R/W
	D2	P0RLD2	Timer0 reload data D2	High	Low	0	R/W
	D1	P0RLD1	Timer0 reload data D1	High	Low	0	R/W
	D0	P0RLD0	Timer0 reload data D0 (LSB)	High	Low	0	R/W
0x1843 Prog. Timer0	D7	P0RLD15	Timer0 reload data D15 (MSB)	High	Low	0	R/W
	D6	P0RLD14	Timer0 reload data D14	High	Low	0	R/W
	D5	P0RLD13	Timer0 reload data D13	High	Low	0	R/W
	D4	P0RLD12	Timer0 reload data D12	High	Low	0	R/W
	D3	P0RLD11	Timer0 reload data D11	High	Low	0	R/W
	D2	P0RLD10	Timer0 reload data D10	High	Low	0	R/W
	D1	P0RLD9	Timer0 reload data D9	High	Low	0	R/W
	D0	P0RLD8	Timer0 reload data D8	High	Low	0	R/W

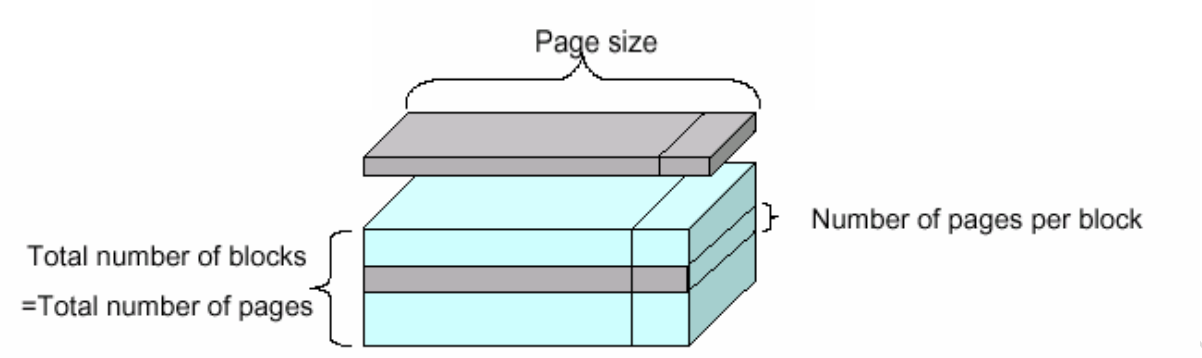
Data [15:0] : programmable timer reload data

Address	Bit	Name	Function	1	0	SR	R/W
0x1844 Prog. Timer0	D7	P0TD7	Timer0 counter data D7	High	Low		R
	D6	P0TD6	Timer0 counter data D6	High	Low		R
	D5	P0TD5	Timer0 counter data D5	High	Low		R
	D4	P0TD4	Timer0 counter data D4	High	Low		R
	D3	P0TD3	Timer0 counter data D3	High	Low		R
	D2	P0TD2	Timer0 counter data D2	High	Low		R
	D1	P0TD1	Timer0 counter data D1	High	Low		R
	D0	P0TD0	Timer0 counter data D0 (LSB)	High	Low		R
0x1845 Prog. Timer0	D7	P0TD15	Timer0 counter data D15 (MSB)	High	Low		R
	D6	P0TD14	Timer0 counter data D14	High	Low		R
	D5	P0TD13	Timer0 counter data D13	High	Low		R
	D4	P0TD12	Timer0 counter data D12	High	Low		R
	D3	P0TD11	Timer0 counter data D11	High	Low		R
	D2	P0TD10	Timer0 counter data D10	High	Low		R
	D1	P0TD9	Timer0 counter data D9	High	Low		R
	D0	P0TD8	Timer0 counter data D8	High	Low		R

Counter data[15:0] : programmable timer counter data, read only

5.9 NAND FLASH CONTROLLER

Internal Configuration of NAND FLASH



Specification Comparison of NAND FLASH

	2MB	4MB	8MB	16MB
Page size	(256+8)Byte	(512+16)Byte	(512+16)Byte	(512+16)Byte
Block size	(4K+128)Byte	(8K+256)Byte	(8K+256)Byte	(16K+512)Byte
Number of page per block	4 pages	8 pages	16 pages	32 pages
Operating voltage	3.0V~3.6V	3.0V~3.6V	3.0V~3.6V	3.0V~3.6V
tPROG	0.25ms Typ.	0.3 ms Typ.	0.2 ms Typ.	0.2 ms Typ.
tBERS	2.0 ms Typ.	2.0 ms Typ.	2.0 ms Typ.	2.0 ms Typ.
TR	10 us Max.	25 us Max.	7 us Max.	10 us Max.
Cycle time	80 ns Min.	50 ns Min.	50 ns Min.	50 ns Min.

	32MB	64MB	128MB(K)	128MB(F)
Page size	(256+8)Byte	(512+16)Byte	(512+16)Byte	(2048+16)Byte
Block size	(4K+128)Byte	(8K+512)Byte	(16K+4k)Byte	(64K+2k)Byte
Number of page per block	64 pages	32 pages	64 pages	64 pages
Operating voltage	3.0V~3.6V	3.0V~3.6V	3.0V~3.6V	3.0V~3.6V
TPROG	0.25ms Typ.	0.20 ms Typ.	0.3ms Typ.	0.3ms Typ.
TBERS	2.0 ms Typ.	2.0 ms Typ.	2.0 ms Typ.	2.0 ms Typ.
TR	10 us Max.	12 us Max.	25 us Max.	25 us Max.
Cycle time	80 ns Min.	50 ns Min.	45 ns Min.	45 ns Min.

	256MB(K)	256MB(F)	512MB(K)	
Page size	(2048+8)Byte	(2048+8)Byte	(2048+8)Byte	
Block size	(128K+4k)Byte	(128K+4k)Byte	(128K+4k)Byte	
Number of page per block	64 pages	64 pages	64 pages	
Operating voltage	3.0V~3.6V	3.0V~3.6V	3.0V~3.6V	
TPROG	0.3ms Typ.	0.3ms Typ.	0.3ms Typ.	
TBERS	2.0 ms Typ.	2.0 ms Typ.	2.0 ms Typ.	
TR	25 us Max.	25 us Max.	25 us Max.	
Cycle time	45 ns Min.	45 ns Min.	45 ns Min.	

Note: 1 Page = 4 Frames = 128 Byte

For NAND Flash

Address	Bit	Name	Function	1	0	SR	R/W
0x1853 NAND FLASH	D7	SMCA7	NAND FLASH column address CA7	High	Low	0	R/W
	D6	SMCA6	NAND FLASH column address CA6	High	Low	0	R/W
	D5	SMCA5	NAND FLASH column address CA5	High	Low	0	R/W
	D4	SMCA4	NAND FLASH column address CA4	High	Low	0	R/W
	D3	SMCA3	NAND FLASH column address CA3	High	Low	0	R/W
	D2	SMCA2	NAND FLASH column address CA2	High	Low	0	R/W
	D1	SMCA1	NAND FLASH column address CA1	High	Low	0	R/W
	D0	SMCA0	NAND FLASH column address CA0	High	Low	0	R/W

D[7:0] : NAND FLASH column address A7-A0

Address	Bit	Name	Function	1	0	SR	R/W
0x1850 NAND FLASH	D7	SMPA7	NAND FLASH page address PA7	High	Low	0	R/W
	D6	SMPA6	NAND FLASH page address PA6	High	Low	0	R/W
	D5	SMPA5	NAND FLASH page address PA5	High	Low	0	R/W
	D4	SMPA4	NAND FLASH page address PA4	High	Low	0	R/W
	D3	SMPA3	NAND FLASH page address PA3	High	Low	0	R/W
	D2	SMPA2	NAND FLASH page address PA2	High	Low	0	R/W
	D1	SMPA1	NAND FLASH page address PA1	High	Low	0	R/W
	D0	SMPA0	NAND FLASH page address PA0	High	Low	0	R/W
0x1851 NAND FLASH	D7	SMPA15	NAND FLASH page address PA15	High	Low	0	R/W
	D6	SMPA14	NAND FLASH page address PA14	High	Low	0	R/W
	D5	SMPA13	NAND FLASH page address PA13	High	Low	0	R/W
	D4	SMPA12	NAND FLASH page address PA12	High	Low	0	R/W
	D3	SMPA11	NAND FLASH page address PA11	High	Low	0	R/W
	D2	SMPA10	NAND FLASH page address PA10	High	Low	0	R/W
	D1	SMPA9	NAND FLASH page address PA9	High	Low	0	R/W
	D0	SMPA8	NAND FLASH page address PA8	High	Low	0	R/W
0x1852 NAND FLASH	D7	SMPA23	NAND FLASH page address PA23	High	Low	0	R/W
	D6	SMPA22	NAND FLASH page address PA22	High	Low	0	R/W
	D5	SMPA21	NAND FLASH page address PA21	High	Low	0	R/W
	D4	SMPA20	NAND FLASH page address PA20	High	Low	0	R/W
	D3	SMPA19	NAND FLASH page address PA19	High	Low	0	R/W
	D2	SMPA18	NAND FLASH page address PA18	High	Low	0	R/W
	D1	SMPA17	NAND FLASH page address PA17	High	Low	0	R/W
	D0	SMPA16	NAND FLASH page address PA16	High	Low	0	R/W

Map for AND Flash

Address	Bit	Name	Function	1	0	SR	R/W
0x1850 AND FLASH	D7	ANDSA7	AND FLASH sector address SA7	High	Low	0	R/W
	D6	ANDSA6	AND FLASH sector address SA6	High	Low	0	R/W
	D5	ANDSA5	AND FLASH sector address SA5	High	Low	0	R/W
	D4	ANDSA4	AND FLASH sector address SA4	High	Low	0	R/W
	D3	ANDSA3	AND FLASH sector address SA3	High	Low	0	R/W
	D2	ANDSA2	AND FLASH sector address SA2	High	Low	0	R/W
	D1	ANDSA1	AND FLASH sector address SA1	High	Low	0	R/W
	D0	ANDSA0	AND FLASH sector address SA0	High	Low	0	R/W
0x1851 AND FLASH	D7	ANDSA15	AND FLASH sector address SA15	High	Low	0	R/W
	D6	ANDSA14	AND FLASH sector address SA14	High	Low	0	R/W
	D5	ANDSA13	AND FLASH sector address SA13	High	Low	0	R/W
	D4	ANDSA12	AND FLASH sector address SA12	High	Low	0	R/W
	D3	ANDSA11	AND FLASH sector address SA11	High	Low	0	R/W
	D2	ANDSA10	AND FLASH sector address SA10	High	Low	0	R/W
	D1	ANDSA9	AND FLASH sector address SA9	High	Low	0	R/W
	D0	ANDSA8	AND FLASH sector address SA8	High	Low	0	R/W

AND Flash Sector Address

Address	Bit	Name	Function	1	0	SR	R/W
0x1853 AND FLASH	D7	ANDCA7	AND FLASH column address CA7	High	Low	0	R/W
	D6	ANDCA6	AND FLASH column address CA6	High	Low	0	R/W
	D5	ANDCA5	AND FLASH column address CA5	High	Low	0	R/W
	D4	ANDCA4	AND FLASH column address CA4	High	Low	0	R/W
	D3	ANDCA3	AND FLASH column address CA3	High	Low	0	R/W
	D2	ANDCA2	AND FLASH column address CA2	High	Low	0	R/W
	D1	ANDCA1	AND FLASH column address CA1	High	Low	0	R/W
	D0	ANDCA0	AND FLASH column address CA0	High	Low	0	R/W
0x185F AND FLASH	D7	ANDWA2	Address write mode: (010: SMSA15-0, 101: SMCA12-0, 111: SMSA15-0 & SMCA11-0)			0	R/W
	D6	ANDWA1				0	R/W
	D5	ANDWA0				0	R/W
	D4	ANDCA12	AND FLASH column address CA12	High	Low	0	R/W
	D3	ANDCA11	AND FLASH column address CA11	High	Low	0	R/W
	D2	ANDCA10	AND FLASH column address CA10	High	Low	0	R/W
	D1	ANDCA9	AND FLASH column address CA9	High	Low	0	R/W
	D0	ANDCA8	AND FLASH column address CA8	High	Low	0	R/W

AND Flash Column Address

For NAND & AND Flash

Address	Bit	Name	Function	1	0	SR	R/W
0x1854 NAND & AND FLASH	D7	SMD7	Read/Write data buffer	High	Low	0	R/W
	D6	SMD6		High	Low	0	R/W
	D5	SMD5		High	Low	0	R/W
	D4	SMD4		High	Low	0	R/W
	D3	SMD3		High	Low	0	R/W
	D2	SMD2		High	Low	0	R/W
	D1	SMD1		High	Low	0	R/W
	D0	SMD0		High	Low	0	R/W

D[7:0] : Data D7-D0 ; command data I/O7-0 at command mode

Address	Bit	Name	Function	1		0		SR	R/W
0x1855 NAND & AND FLASH	D5	ISMXCD	Card detect on interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D4	ISMXBY	Busy end interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D3	ISMEND	NAND FLASH finish interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D2	EISMXCD	Card detect interrupt mask register	Enable		Mask		0	R/W
	D1	EISMXBY	Ready/busy interrupt mask register	Enable		Mask		0	R/W
	D0	EISMEND	Block finish interrupt mask register	Enable		Mask		0	R/W

D5 : card detect on interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D4 : busy end interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D3 : data read finish interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D2 : card detect on interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

D1 : busy end interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

D0 : Block data read finish interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

Address	Bit	Name	Function	1	0	SR	R/W
0x1856 NAND & AND FLASH	D7	ENSM	Chip Select on/off	On	Off	0	R/W
	D6						
	D5	SMRUN	Interface run	Run	None		W
	D4						
	D3	FOEL	Force AND Flash OE Low	Force Low	Normal	0	R/W
	D2	FCH	Force AND Flash CDE High	Force High	Normal	0	R/W
	D1	SMOP1	Operating mode select	0 : command 1 : address write	2 : data write 3 : data read	00	R/W
	D0	SMOP0					

D7 : Chip Select on/off , 0 = off, 1 = on

D5 : Run, 0 = None, 1 = run

D[1:0] : Operating mode select, 0 = command, 1 = address write, 2 = data write, 3 = data read

Address	Bit	Name	Function	1	0	SR	R/W
0x1857 NAND & AND FLASH	D7	SMAM	Access Method	By hardware	By CPU	0	R/W
	D6	SMCLK2	Data rate select	000 : clock/2 001 : clock/4 010 : clock/8 011 : clock/16	100 : clock/32 101 : clock/64 110 : clock/128 111 : clock/256	000	R/W
	D5	SMCLK1					
	D4	SMCLK0					
	D3	SMBKL	Data Transfer Block Length	Block Length = 2^SMBKL BKL=0 ~ 12		0	R/W
	D2						
	D1						
	D0						

D7 : Access Method. 1 : By hardware, 0 : By CPU.

D[6:4] : Data rate select, 0 = clock/2, 1 = clock/4, 2 = clock/8, 3 = clock/16, 4 = clock/32, 5 = clock/64, 6 = clock/128 7 = clock/256

D[3:0] : Data transfer length, block length = SMBKL + 1

Address	Bit	Name	Function	1	0	SR	R/W
0x1858 NAND & AND FLASH	D7						
	D6						
	D5	ODD	Odd or even	Odd	Even	0	R/W
	D4						
	D3						
	D2						
	D1	MODE	Read or write	write	read	0	R/W
	D0	STC	ECC start	start	stop	0	R/W
0x1859 NAND & AND FLASH	D7	LP7A	ECC function	High	Low	0	R
	D6	LP6A	ECC function	High	Low	0	R
	D5	LP5A	ECC function	High	Low	0	R
	D4	LP4A	ECC function	High	Low	0	R
	D3	LP3A	ECC function	High	Low	0	R
	D2	LP2A	ECC function	High	Low	0	R
	D1	LP1A	ECC function	High	Low	0	R
	D0	LP0A	ECC function	High	Low	0	R
0x185A NAND & AND FLASH	D7	LP15A	ECC function	High	Low	0	R
	D6	LP14A	ECC function	High	Low	0	R
	D5	LP13A	ECC function	High	Low	0	R
	D4	LP12A	ECC function	High	Low	0	R
	D3	LP11A	ECC function	High	Low	0	R
	D2	LP10A	ECC function	High	Low	0	R
	D1	LP9A	ECC function	High	Low	0	R
	D0	LP8A	ECC function	High	Low	0	R
0x185B NAND & AND FLASH	D7	CP5A	ECC function	High	Low	0	R
	D6	CP4A	ECC function	High	Low	0	R
	D5	CP3A	ECC function	High	Low	0	R
	D4	CP2A	ECC function	High	Low	0	R
	D3	CP1A	ECC function	High	Low	0	R
	D2	CP0A	ECC function	High	Low	0	R
	D1	ECCT1A	When odd is true, ECCT1A=1	Odd	Even	0	R
	D0	ECCT0A	When odd is true, ECCT0A=1	Odd	Even	0	R

Address	Bit	Name	Function	1	0	SR	R/W
0x185C NAND & AND FLASH	D7	LP7B	ECC function	High	Low	0	R
	D6	LP6B	ECC function	High	Low	0	R
	D5	LP5B	ECC function	High	Low	0	R
	D4	LP4B	ECC function	High	Low	0	R
	D3	LP3B	ECC function	High	Low	0	R
	D2	LP2B	ECC function	High	Low	0	R
	D1	LP1B	ECC function	High	Low	0	R
	D0	LP0B	ECC function	High	Low	0	R
0x185D NAND & AND FLASH	D7	LP15B	ECC function	High	Low	0	R
	D6	LP14B	ECC function	High	Low	0	R
	D5	LP13B	ECC function	High	Low	0	R
	D4	LP12B	ECC function	High	Low	0	R
	D3	LP11B	ECC function	High	Low	0	R
	D2	LP10B	ECC function	High	Low	0	R
	D1	LP9B	ECC function	High	Low	0	R
	D0	LP8B	ECC function	High	Low	0	R
0x185E NAND & AND FLASH	D7	CP5B	ECC function	High	Low	0	R
	D6	CP4B	ECC function	High	Low	0	R
	D5	CP3B	ECC function	High	Low	0	R
	D4	CP2B	ECC function	High	Low	0	R
	D3	CP1B	ECC function	High	Low	0	R
	D2	CP0B	ECC function	High	Low	0	R
	D1	ECCT1B	When odd is true, ECCT1B=1	Odd	Even	0	R
	D0	ECCT0B	When odd is true, ECCT0B=1	Odd	Even	0	R

0x1858 ~ 0x185E : ECC function

Address	Bit	Name	Function	1	0	SR	R/W
0x185F NAND FLASH	D7	SMWA2	Address write mode (000: SMPA20-0 & SMCA7-0; 010: SMPA15-0 & SMCA7-0; 100: SMPA20-SMPA0; 110: SMPA15-SMPA0; 001: SMPA20-0 & SMCA11-0; 011: SMPA20-0 & SMCA15-0); 100&110 only use at Block Erase command			00	R/W
	D6	SMWA1					
	D5	SMWA0					
	D4	SMCA12	NAND FLASH column address CA12	High	Low	0	R/W
	D3	SMCA11	NAND FLASH column address CA11	High	Low	0	R/W
	D2	SMCA10	NAND FLASH column address CA10	High	Low	0	R/W
	D1	SMCA9	NAND FLASH column address CA9	High	Low	0	R/W
	D0	SMCA8	NAND FLASH column address CA8	High	Low	0	R/W

D[7:5] : address write mode, 0 = 4 bytes (SMPA20-0 & SMCA7-0), 2 = 3 bytes (SMPA15-0 & SMCA7-0), 4 = 3 bytes (SMPA20-SMPA0), 6 = 2 byte (SMPA15-SMPA0), 1 = 5 bytes (SMPA20-0 & SMCA11-0), 3 = 4 bytes (SMPA20-0 & SMCA15-0),

D[4:0] : NAND FLASH column address SMCA12-SMCA8

5.9.1 NAND FLASH COMMAND & STATUS

NAND FLASH has address multiplexed into 8 I/O's. This scheme reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing XWE to low while XCE is low. Data is latched on the rising edge of XWE. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except for Block Erase command which requires two cycles: one cycle for erase-setup and another for erase-execution after block address loading. For the 4MB ~ 32MB physic space requires 25 addresses, thereby requiring three cycles for byte- level addressing: column address, low page address, high page address. The 64MB or 128MB or 256MB or 512MB physic space needs 26 or (K:27 & F:28) or 29 or 30 addresses, thereby requiring four cycles for byte-level addressing. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase operation, however, only two page address cycles are used. Device operations are selected by writing specific command register.

The specific commands as follows:

Function	1st cycle	2nd cycle	Acceptable command during Busy	Pointer position
Sequential Data Input	80H			
Read Mode 1	00H			0~255 bytes @ K9D5608V0M 0~511 bytes @ TH58512DC
Read Mode 2	01H			256~511 bytes @ K9D5608V0M 0~511 bytes @ TH58512DC
Read Mode 3	50H			512~527 bytes
Read ID	90H			
Reset	FFH		yes	
Page Program	10H			
Block Erase	60H	D0H		
Read Status	70H		yes	

The 128M(K) specific commands as follows:

Function	1st cycle	2nd cycle	3nd cycle	Acceptable command during Busy
Read 1	00H/01H			
Read 2	50H			
Read ID	90H			
Reset	FFH		yes	yes
Page program(true)	80H	10H		
Page program(dummy)	80H	11H		
Copy-Back Program(true)	00H	8AH	10H	
Copy-Back Program(dummy)	03H	8AH	11H	
Block Erase	60H	D0H		
Multi-plane block erase	60H	D0H		
Read status	70H			yes
Read multi-plane status	71H		yes	yes

The 128M(F), 256M, 512M specific commands as follows:

Function	1st cycle	2nd cycle	Acceptable command during Busy	Pointer position
Read	00H	30H		
Read for Copy Back	00H	35H		
Read ID	90H			
Reset	FFH		yes	
Page program	80H	10H		
Cache program	80H	15H		
Copy-Back Program	85H	10H		
Block Erase	60H	D0H		
Random Data Input	85H			
Random Data Output	05H	E0H		
Read Status	70H		yes	

The status register definition as follow:

SR	Status	Definition
I/O0	Program/Erase	0 : Successful ; 1 : Error
I/O1-I/O5	Reserved	0
I/O6	Device Operation	0 : Busy ; 1 : Ready
I/O7	Write Protect	0 : Protected ; 1: not Protected

5.9.2 PIN DESCRITION

NAND FLASH I/O Pin Assignment

Command Latch Enable(CLE)

The CLE input controls the path activation for commands sent to the command register. When active HIGH, commands are latched into the command register through the I/O ports on the rising edge of the XWE signal

Address Latch Enable(ALE)

The ALE input controls the path activation for address and input data to the internal address/data register. Addresses are latched on the rising edge of XWE with ALE high, and input data is latched when ALE is low

Chip Enable(XCE)

The XCE input is the device selection control. When XCE goes high during a read operation the device is returned to standby mode. However, when the device is in the busy state during program or erase, XCE high is ignored and does not return the device to standby mode

Write Enable (XWE)

The XWE input controls writes to the I/Os port, commands, address and data are latched on the rising edge of the XWE pulse.

Read Enable(XRE)

The /RE is the serial data-out control and when active drives the data on the I/O bus. Data is valid after the falling edge of XRE which also increments internal column address counter by one.

Write Protect(XWP)

The XWP pin provides inadvertent write/erase operation during power transitions. The internal high voltage generator is disabled when XWP pin is active low.

Ready/Busy(RB)

The RB output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and return to high state upon completion. It is an open drain output and does not float to high impedance condition when chip is deselect or outputs are disabled

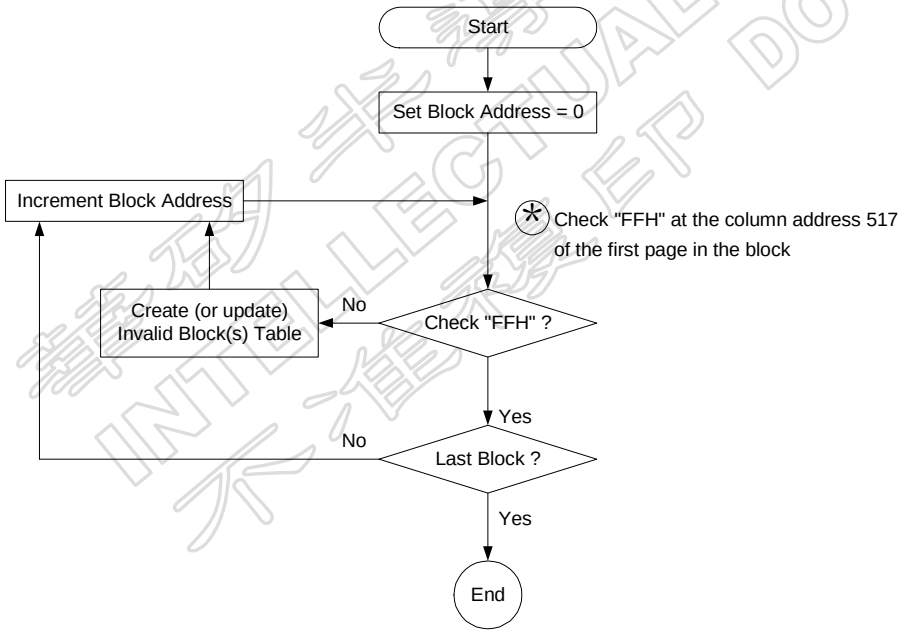
I/O port (I/O0~I/O7)

The I/O port is used to input command, address and data, and to output data during read operation. The I/O port float to high impedance condition when chip is deselect or outputs are disabled

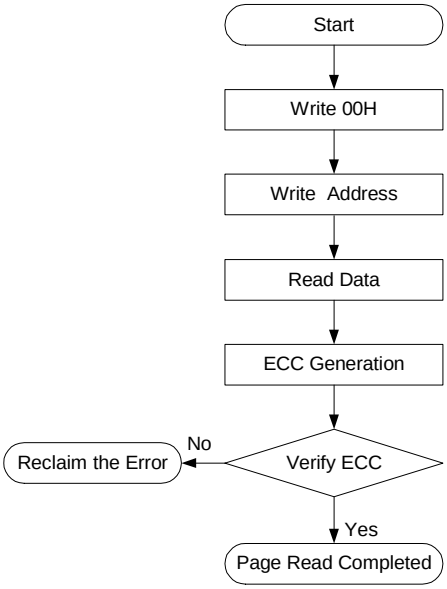
5.9.3 NAND FLASH PROGRAM FLOW CHART

The flow of command will descript as follow diagram:

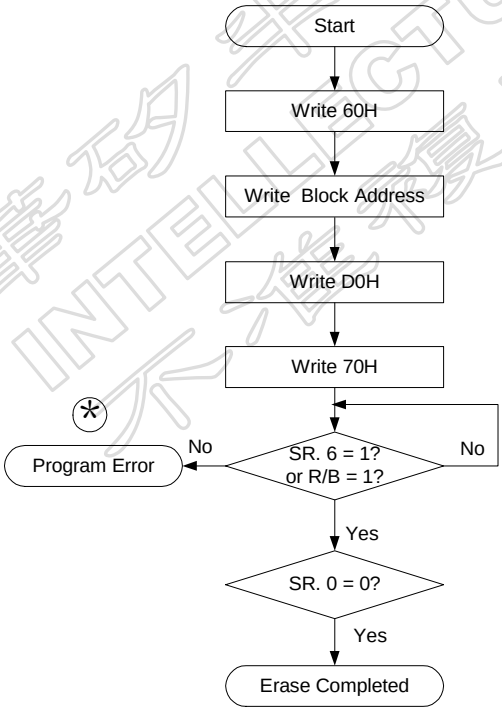
Identifying Invalid Block(s)



Read Flow Chart

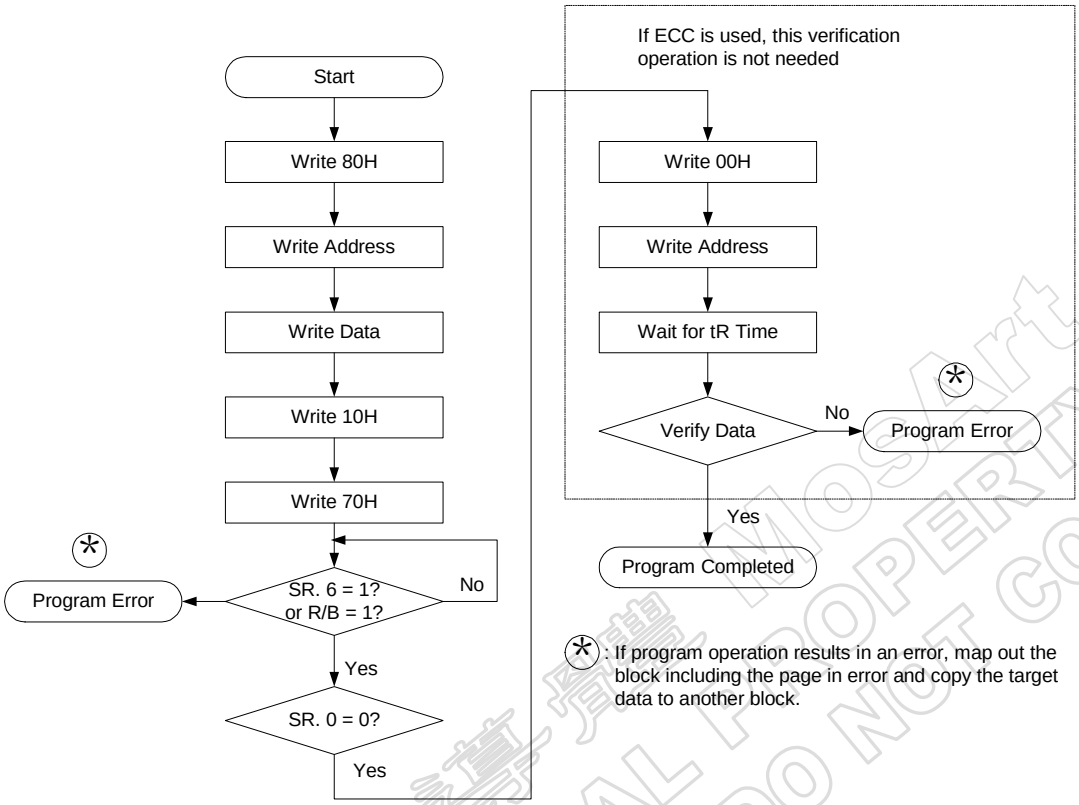


Erase Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

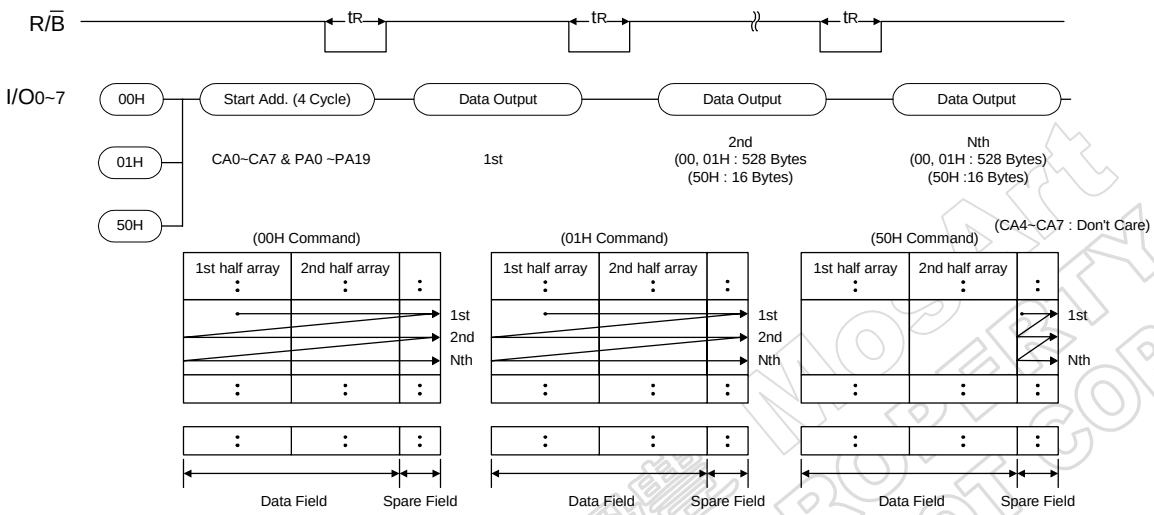
Program Flow Chart



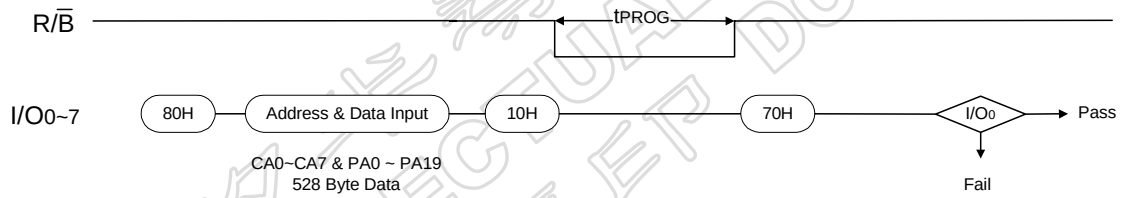
5.9.4 NAND FLASH OPERATION TIMING

The timing of command will descript as follow diagram:

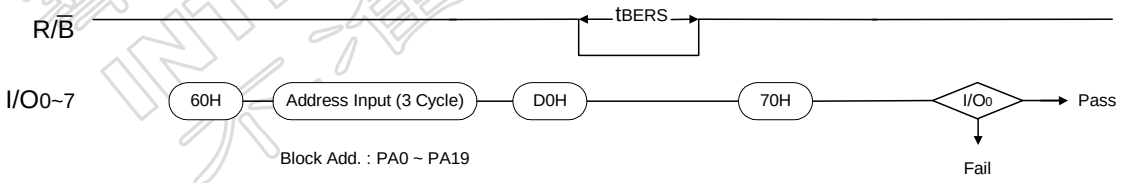
Sequential Row Read Operation



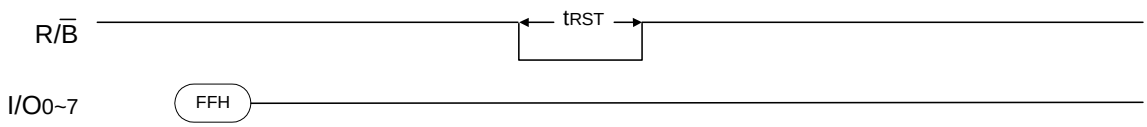
Program & Read Status Operation



Block Erase Operation



RESET Operation



5.10 SECURE DIGITAL (SD) MEMORY CARD CONTROLLER

The SD (Secure Digital) Memory Card, jointly developed by Toshiba Corp., Matsushita Electric Industrial Co., Ltd., and SanDisk Corp. (U.S.A.), is a new card-type medium. The SD Memory Card is a safe storage medium suitable for commercial content that requires robust copyright protection SD memory cards are next generation memory devices that offer an incredible combination of high storage capacity (currently 16, 32 and 64 MB), fast data transfer rates, great flexibility and excellent security — all in a memory card about the size of a postage stamp! SD memory cards are non-volatile, which means they do not require power to retain the information stored on them. They are solid-state devices, so they have no moving parts to skip or break down. And they will revolutionize information, entertainment and communications by putting advanced digital storage technology quite literally at your fingertips

Key features of SD memory card

- ✧ Average 2MB/s data transfer rate (10MB/s in near future)
- ✧ SDMI Portable Media (PM) Security Compliant
- ✧ Interface Protection Channels - Higher ESD tolerance
- ✧ Write Protect switch on card casing
- ✧ SD Host allows MultiMediaCard upward compatibility
- ✧ 3C(Toshiba, Matsushita, SanDisk) excellent alliance
- ✧ SD Association to standardize the specifications and promote global adoption

SD Card I/O Pin Assignment

Key Features of MA8201-H72 Secure Digital Memory Controller

- Support 1-bit and 4-bit mode
- Support SD bus mode
- Programmable clock source
- Automatic CRC generation and check
- Automatic Interrupt Generation

Address	Bit	Name	Function	1		0		SR	R/W
0x1860 SD card	D7	SOP	Start operation	R	Running	R	Idle	0	R/W
				W	Start	W	None	0	R/W
	D6	STOP	Stop operation	Stop		None		0	W
	D5	GNR	Get next response (only for command R136 bits mode)	Get Next Response		None		0	W
	D4	COM	Command operation mode	11: R136-Bit Mode 10:Normal Mode		01: No Response 00: No Action		0	R/W
	D3							0	R/W
	D2	BM	Bit Mode	4 Bits Mode		1 Bit Mode		0	R/W
	D1	GENR00	Data operation mode	11: Write Data 10: Read Data		0x: No Action		0	R/W
	D0							0	R/W

D7 : SD start trigger, Read 0=idle, 1=running, Write 0=none, 1=start

D6: SD stop operation, Write 0=None, 1=Stop

D5: Get next response, Write 0=None 1=Get next response

D[4:3] : SD command operation mode, 00=No action, 01=No Response Mode
01=Normal Mode, 11=R136 Bits Mode

D2: SD bit mode selection, Write only, 1=4-bit mode, 0=1-bit mode

D[1:0] : SD data operation mode 0X=No action, 10=Read data, 11=Write data

Address	Bit	Name	Function	1		0		SR	R/W
0x1861 SD card	D7	RIF	SD response interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D6	BRIF	SD block read finished interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D5	BWIF	SD block write finished interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D4	OBRWIF0	SD one byte R/W finished interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D3	CRCE	Status: CRC7 error	Yes		No		0	R
	D2	BWUS	Status: CRC16 error	Yes		No		0	R
	D1	FE	Status: block write unsuccessful r	Yes		No		0	R
	D0	IM	SD interrupt mask register	Enable		Mask		0	R/W

D7: SD response interrupt factor flag , read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D6: SD block read finished interrupt factor flag , read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D5: SD block write finished interrupt factor flag , read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D4: SD one byte R/W finished interrupt factor flag , read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D3 : SD command response CRC error, read 0 = no error, 1 = error

D2 : SD Data Block Read CRC error, read 0 = no error, 1 = error

D1 : SD Block Write CRC Status Error, read 0 = no error, 1 = error

D0 : SD interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

Address	Bit	Name	Function	1	0	SR	R/W
0x1862 SD card	D7	SDAM	Access Method	By hardware	By CPU	0	R/W
	D6	CLKS	SD Clock Select	111: /256 110: /128 101: /64 100: /32	011: /16 010: /8 001: /4 000: /2	0	R/W
	D5					0	R/W
	D4					0	R/W
	D3	BKL	Read/Write Block Length	Block Length = 2^BKL BKL = 0 ~ 11		0	R/W
	D2					0	R/W
	D1					0	R/W
	D0					0	R/W

D7 : Access Method. 1 : By hardware, 0 : By CPU.

D[6:4]: SD module clock selection

000=divided by 2, 001=divided by 4, 010=divided by 8, 011=divided by 16

100=divided by 32, 101=divided by 64, 110=divided by 128, 111=divided by 256

D[3:0]: SD read/write block Length = 2^BKL BKL ranges in 0 ~11

BKL = 0000 1 Byte

BKL = 0001 2 Bytes

BKL = 0010 4 Bytes

BKL = 0011 8 Bytes

..

.

BKL =1011 2048 Bytes

Address	Bit	Name	Function	1	0	SR	R/W
0x1863 0x1864 0x1865 0x1866 0x1867 SD card	D7	SDCMD	Write: Command Bit 47 ~ 8 Read: Normal Mode or R136 Bits Mode	High	Low	0	R/W
	D6	SDCMD		High	Low	0	R/W
	D5	SDCMD		High	Low	0	R/W
	D4	SDCMD		High	Low	0	R/W
	D3	SDCMD		High	Low	0	R/W
	D2	SDCMD		High	Low	0	R/W
	D1	SDCMD		High	Low	0	R/W
	D0	SDCMD		High	Low	0	R/W

SDCMD[47:8] : command data bits

SD controller contains 40 bits command buffer to store SD standard command format Bit 48 ~ 8 and uses the same buffer to store the response. It also uses 32 bits data buffer to improve the efficiency of transmitting/receiving. SD controller provides three command operation modes and two data operation modes. Details registers function and usage will be presented and discussed in following program flow section.

Address	Bit	Name	Function	1	0	SR	R/W
0x1868 SD card	D7	SDRWB	Data Read/Write Buffer	High	Low	0	R/W
	D6	SDRWB		High	Low	0	R/W
	D5	SDRWB		High	Low	0	R/W
	D4	SDRWB		High	Low	0	R/W
	D3	SDRWB		High	Low	0	R/W
	D2	SDRWB		High	Low	0	R/W
	D1	SDRWB		High	Low	0	R/W
	D0	SDRWB		High	Low	0	R/W

SDRWB[63:0] : SD data read/write buffer

Address	Bit	Name	Function	1	0	SR	R/W
0x1869 SD card	D2						
	D1	SDWUNB	Wait Until Not Busy(Only for R1b)	Wait	No	0	W
	D0	SDBUSY	Busy Flag (DATA 0)	Not Busy	Busy	1	R

SDWUNB: AT the response R1b, wait until DATA 0 is not busy.

SDBUSY: DATA 0 indicates busy state

5.10.1 PROGRAM FLOW

Before discussing these various cases, programmers must know the three registers setting below:

1. SD module clock selection (0x1862 CLKS):
   In the Card Identification Mode, the clock must be less than 400K. After identifying all the cards connected to host, programmers can decide adequate clock speed to transfer data,
2. Bit Mode (0x1862 BM):
   After power up, by default, the SD Card will use only DAT0 for data transfer. It means 1-bit mode is used. After initialization programmers can change the bus width to 4-bit mode.
3. Read/Write Block Length (0x1862 BKL):
   After identifying the card connected to host, programmers can decide the block length for data transfer.

Following cases are typical types of transactions:

Case A: A command with no response.

1. Write the command content into registers CMDRPD (0x1863 ~ 0x1867), programmers needn't give the command frame Bit 7 ~ 0 (CRC and End bit) because hardware will generate them automatically.
2. Enable interrupt IM (0x1861 Bit 0).
3. Choose Command Operation Mode = 01 (No response mode), Data Operation Mode=00 (No action), and Start operation. The above setting means writing 0x88 into register 0x1860.
4. Wait the interrupt generation.
5. Check RIF (0x1861 Bit 7), it must be one. Then write one into this bit to clear interrupt.

Case B: A command with 48 bits response (R1, R1b, R3, R6).

1. Write the command content into registers CMDRPD (0x1863 ~ 0x1867), programmers needn't give the command frame Bit 7 ~ 0 (CRC and End bit) because hardware will generate them automatically.
2. Enable interrupt IM (0x1861 Bit 0).
3. Choose Command Operation Mode = 10 (Normal mode), Data Operation Mode=00 (No action), and Start operation. The above setting means writing 0x90 into register 0x1860.
4. Wait the interrupt generation.
5. Check RIF (0x1861 Bit 7), it must be one. Then write one into this bit to clear interrupt.
6. Check CRCE7 (0x1861 Bit 3). If there is a CRC error, retry this command again. If this bit is zero, the transaction is successful
7. Read response from registers CMDRPD (0x1863 ~ 0x1867). They present response format from bit 47 to bit 8. CRC are checked by hardware and reflect at the bit CRCE7 (0x1861 Bit 3).

Case C: A command with 136 bits response (R2).

1. Write the command content into registers CMDRPD (0x1863 ~ 0x1867), programmers needn't give the command frame Bit 7 ~ 0 (CRC and End bit) because hardware will generate them automatically.
2. Enable interrupt IM (0x1861 Bit 0).
3. Choose Command Operation Mode = 11 (R136 Bits mode), Data Operation Mode=00 (No action), and Start operation. The above setting means writing 0x98 into register 0x1860.
4. Wait the interrupt generation.
5. Check RIF (0x1861 Bit 7), it must be one. Then write one into this bit to clear interrupt.
6. Read response from registers CMDRPD (0x1863 ~ 0x1867). They present response format from bit 135 to bit 96
7. Write one into GNR (0x1860 Bit 5) to get other response bits. It is NOT necessary to set SOP (0x1860 Bit 7) to be one. The recommended data written into 0x1860 is 0x38.
8. Wait the interrupt generation
9. Check RIF (0x1861 Bit 7), it must be one. Then write one into this bit to clear interrupt
10. Read response from registers CMDRPD (0x1863 ~ 0x1867). They present response format from bit 95 to bit 56.
11. Write one into GNR (0x1860 Bit 5) to get other response bits. It is NOT necessary to set SOP (0x1860 bit 7) to be one. The recommended data written into 0x1860 is 0x38.
12. Wait the interrupt generation
13. Check RIF (0x1861 Bit 7), it must be one. Then write one into this bit to clear interrupt
14. Read response from registers CMDRPD (0x1863 ~ 0x1867). They present response format from bit 55 to bit 16.
15. Write one into GNR (0x1860 Bit 5) to get other response bits. It is NOT necessary to set SOP (0x1860 bit 7) to be one. The recommended data written into 0x1860 is 0x38.
16. Wait the interrupt generation
17. Check RIF (0x1861 Bit 7), it must be one. Then write one into this bit to clear interrupt.
18. Read response from registers CMDRPD 0x1867. They present response format from bit 15 to bit 8. CRC are checked by hardware and reflect at the bit CRCE7 (0x1861 Bit 3).
19. Check CRCE7 (0x1861 Bit 3). If there is a CRC error, retry this command again. If this bit is zero, the transaction is successful

Case D: A read data transaction.

1. Firstly programmers must select one card for data read operation by CMD7, and set the valid block length for block oriented data transfer by CMD16.
2. Write block length into register 0x1862 BKL.
3. Choose 1-Bit mode or 4-Bits mode (0x1862 BM).
4. Enable interrupt IM (0x1861 Bit 0).
5. Write the block read command content (CMD17) into registers CMDRPD (0x1863 ~ 0x1867), programmers needn't give the command frame Bit 7 ~ 0 (CRC and End bit) because hardware will generate them automatically
6. The CMD17 will get the bock data. Because it is possible that data will be sent out on the data bus by SD card in the response stage of this command, programmers MUST set both command operation mode=10 and data operation mode=10. The above setting means writing 0x92 into register 0x1860.
7. Wait the interrupt generation.
8. Check RIF (0x1861 Bit 7). If it is one, write one into this bit to clear interrupt. Then check CRCE7 (0x1861 Bit 3). Note this flag maybe occur later than OTRWIF flag if SD card sends out data quickly.
9. Because the data buffers are one byte, a block must be read in several times if the block length is larger than 1 byte.
10. Programmers must check BRIF and OTRWIF (0x1861 Bit 6 and Bit 4). If OTRWIF is one, write one to this bit to clear interrupt. Then read data form DRWB (0x1868). This read action will trigger next read operation of other bytes of the block. Go to step 7.
11. If BRIF is one, write one to this bit to clear interrupt. Then read one byte form DRWB (0x1868). This flag means a block read has finished. Programmers may check CRCE16 (0x1861 Bit 2) to know if the data are valid. If more blocks will be read, go to step 13,
12. Stop read transaction by CMD12. Please follow processes of Case B. (This step should be skip if Single block read). Some SD cards will negate DATA 0 after receiving STOP (CMD12) command. . Because the response mode of CMD12 is R1b, be sure to set 0x1869 Bit1 (SDWUNB) to 1. This bit will be cleared by hardware automatically after CMD 12 is finished.
13. Set command operation mode=00 (No action) and data operation mode=10. The above setting means writing 0x82 into register 0x1860. Then go to step 7.

Case E: A write data transaction.

1. Firstly programmers must select one card for data write operation by CMD7, and set the valid block length for block data transfer by CMD16.
2. Write block length into register 0x1862 BKL.
3. Choose 1-Bit mode or 4-Bits mode (0x1862 BM).
4. Enable interrupt IM (0x1861 Bit 0).
5. Write the block write command content (CMD24) into registers CMDRPD (0x1863 ~ 0x1867), please follow processes of Case B to finish this command.
6. Set command operation mode=00 and data operation mode=11. The above setting means writing 0x83 into register 0x1860.
7. Because the data buffers are one byte, a block must be written in several times if the block length is larger than 1 byte. Write the data into DRWB (0x1868).
8. Wait the interrupt generation.
9. Check BWIF and OTRWIF (0x1861 Bit 5 and Bit 4).
10. If OTRWF is one, write one to this bit to clear interrupt. Then write next byte into DRWB (0x1868 ~ 0x186F). This action will trigger write operation of other bytes of the block. Go to step 8.
11. If BWIF is one, write one to this bit to clear interrupt. This flag means a block write has finished. Programmers may check BWUS (0x1861 Bit 1) to know if the data write are successful. 'One' means unsuccessful and 'zero' means successful. If multiple block will be written, go to step 7,
12. Stop write transaction by CMD12. Please see follow processes of Case B. (Note: The step should be skip if Single block write)
13. Some SD cards will negate DATA 0 after receiving STOP (CMD12) command. . Because the response mode of CMD12 is R1b, be sure to set 0x1870 Bit1 (SDWUNB) to 1. This bit will be cleared by hardware automatically after CMD 12 is finished.

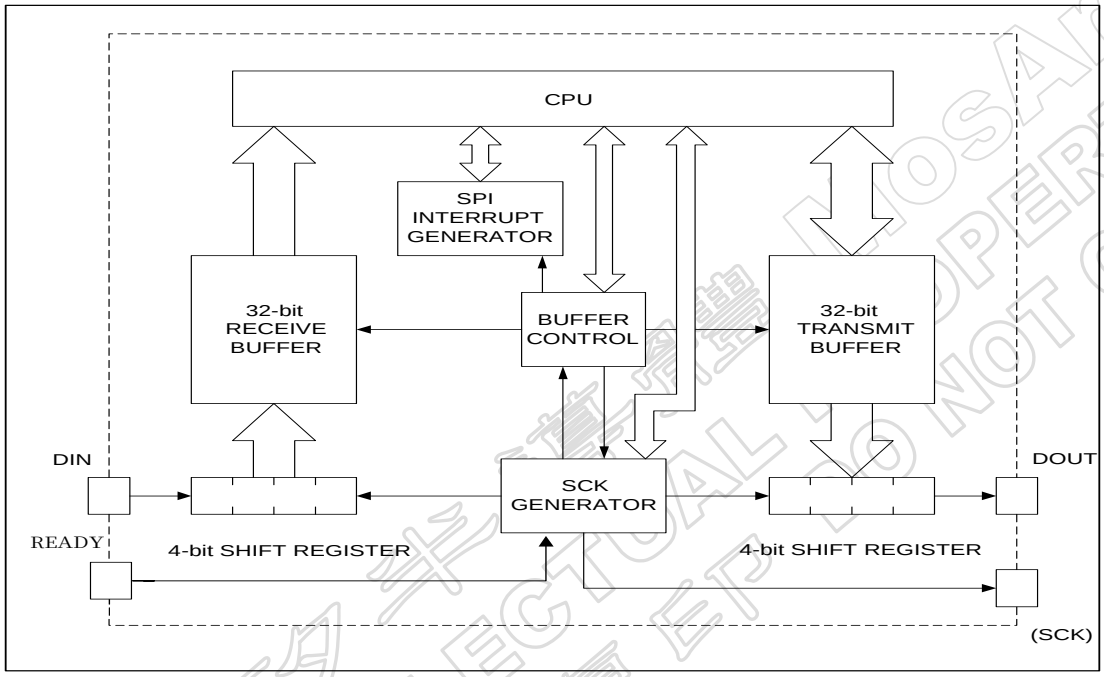
Command Flow example

1. CMD0 (Case A)
2. CMD0 (Case A)
3. CMD0 (Case A)
4. CMD55;ACMD41 (Case B; Case B)
5. CMD55;ACMD41 (Case B; Case B)
6. CMD2 (Case C)
7. CMD3 (Case B)
8. CMD9 (Case C)
9. CMD7 (Case B)
10. CMD55,ACMD51 (Case B; Case D block length = 8 bytes)
11. CMD55,ACMD6 (Case B; Case B)
12. CMD16 (Case B)
13. CMD24 or CMD 25 (Case E)
14. CMD 12 (Case B) (Skip if CMD 24)
15. CMD 17 or CMD 18 (Case D)
16. CMD 12 (Case B) (Skip if CMD 17)

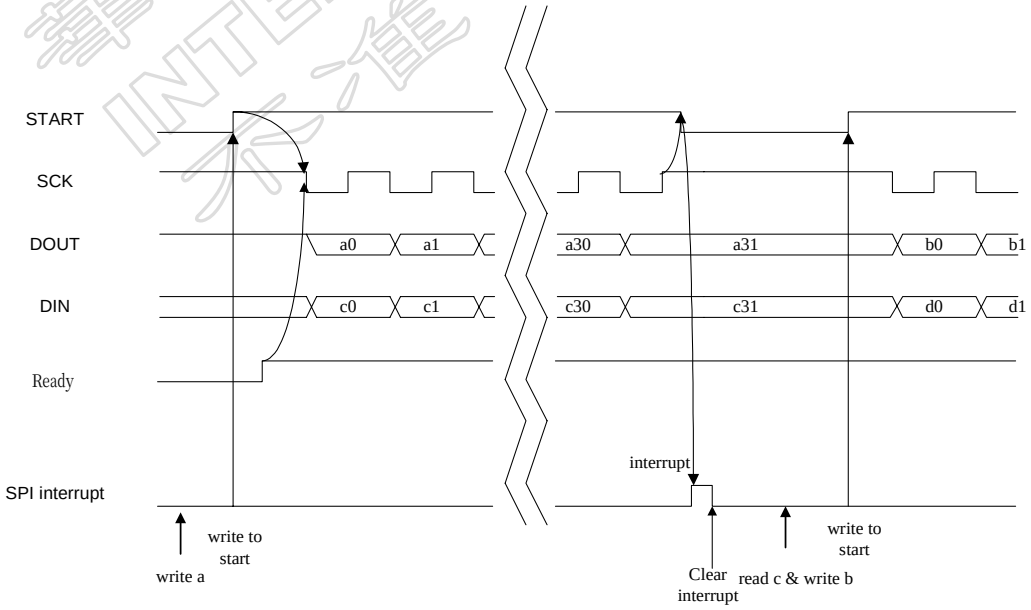
5.11 SERIAL PERIPHERAL INTERFACE

The MA8201-H72 has one Serial Peripheral Interface (SPI) for data transfer within MCU and peripherals. By configuring I/O port 0 as SPI port, the built-in data buffer can automatically and continuously transfer up to 32 bits of data. The SPI can interface with various type of external devices that requires serial data transfer.

SPI Block Diagram



SPI Timing Diagram



Address	Bit	Name	Function	1	0	SR	R/W
0x1880 SPI	D7	SPID7	SPI transmit/receive data bit 7	High	Low	0	R/W
	D6	SPID6	SPI transmit/receive data bit 6	High	Low	0	R/W
	D5	SPID5	SPI transmit/receive data bit 5	High	Low	0	R/W
	D4	SPID4	SPI transmit/receive data bit 4	High	Low	0	R/W
	D3	SPID3	SPI transmit/receive data bit 3	High	Low	0	R/W
	D2	SPID2	SPI transmit/receive data bit 2	High	Low	0	R/W
	D1	SPID1	SPI transmit/receive data bit 1	High	Low	0	R/W
	D0	SPID0	SPI transmit/receive data bit 0	High	Low	0	R/W
0x1881 SPI	D7	SPID15	SPI transmit/receive data bit 15	High	Low	0	R/W
	D6	SPID14	SPI transmit/receive data bit 14	High	Low	0	R/W
	D5	SPID13	SPI transmit/receive data bit 13	High	Low	0	R/W
	D4	SPID12	SPI transmit/receive data bit 12	High	Low	0	R/W
	D3	SPID11	SPI transmit/receive data bit 11	High	Low	0	R/W
	D2	SPID10	SPI transmit/receive data bit 10	High	Low	0	R/W
	D1	SPID9	SPI transmit/receive data bit 9	High	Low	0	R/W
	D0	SPID8	SPI transmit/receive data bit 8	High	Low	0	R/W
0x1882 SPI	D7	SPID23	SPI transmit/receive data bit 23	High	Low	0	R/W
	D6	SPID22	SPI transmit/receive data bit 22	High	Low	0	R/W
	D5	SPID21	SPI transmit/receive data bit 21	High	Low	0	R/W
	D4	SPID20	SPI transmit/receive data bit 20	High	Low	0	R/W
	D3	SPID19	SPI transmit/receive data bit 19	High	Low	0	R/W
	D2	SPID18	SPI transmit/receive data bit 18	High	Low	0	R/W
	D1	SPID17	SPI transmit/receive data bit 17	High	Low	0	R/W
	D0	SPID16	SPI transmit/receive data bit 16	High	Low	0	R/W
0x1883 SPI	D7	SPID31	SPI transmit/receive data bit 31	High	Low	0	R/W
	D6	SPID30	SPI transmit/receive data bit 30	High	Low	0	R/W
	D5	SPID29	SPI transmit/receive data bit 29	High	Low	0	R/W
	D4	SPID28	SPI transmit/receive data bit 28	High	Low	0	R/W
	D3	SPID27	SPI transmit/receive data bit 27	High	Low	0	R/W
	D2	SPID26	SPI transmit/receive data bit 26	High	Low	0	R/W
	D1	SPID25	SPI transmit/receive data bit 25	High	Low	0	R/W
	D0	SPID24	SPI transmit/receive data bit 24	High	Low	0	R/W

SPI transmit/receive data bit [31:0]

Address	Bit	Name	Function	1		0		SR	R/W
0x1884 SPI	D7								
	D6	SPICLK	SPI clock initial level select	High level		Low level		0	R/W
	D5	SPICR	Check Ready to start	Yes		No		1	R/W
	D4	SPIRUN	SPI transfer start indication	R W	Doing Start	R W	Over None	0	R/W
	D3	SPITMD1	Select which nibble to transmit first	Highest		Lowest		0	R/W
	D2	SPITMD0	Select which bit to transmit first	MSB		LSB		0	R/W
	D1	SPIRMD1	Select which nibble to store first	Highest		Lowest		0	R/W
	D0	SPIRMD0	Select which bit to store first	MSB		LSB		0	R/W

D6 : SPI clock initial level select 0=Low level, 1=High level

D5 : SPI check Ready to start 0=No, 1=Yes

D4 : SPI transfer start indication Read 0=Finished, 1=Doing, Write 0=None 1=Start

D3 : SPI select which nibble to transmit first 0:Lowest, 1=Highest

D2 : SPI select which bit to transmit first, 0=LSB, 1=MSB

D1 : SPI select which nibble to store first 0:Lowest, 1=Highest

D0 : SPI select which bit to store first, 0=LSB, 1=MSB

Address	Bit	Name	Function	1		0		SR	R/W
0x1885 SPI	D7	SPIF	SPI interrupt factor flag	R W	Yes Reset	R W	No None	0	R/W
	D6	SPIM	SPI interrupt mask register	Enable		Mask		0	R/W
	D5	SPISIZE1	SPI data length select	11: 32bits 10:24bits		01:16bits 00:8bits		0	R/W
	D4	SPISIZE0						0	R/W
	D3	SPICK3	SPI clock frequency select	Select range n = 0 ~ 12 SPICLK = CPU clock / 2 ^(n+1) For instance, n=4 SPICLK = CPU clock / 32				0	R/W
	D2	SPICK2						0	R/W
	D1	SPICK1						1	R/W
	D0	SPICK0						0	R/W

D7 : SPI interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D6 : SPI interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

D[5:4] : SPI data length select, 0 = 8-bit, 1=16-bit, 2=24-bit, 3=32-bit data

D[3:0] : SPI clock frequency select, SPICLK = CPU clock / 2 ^(n+1).

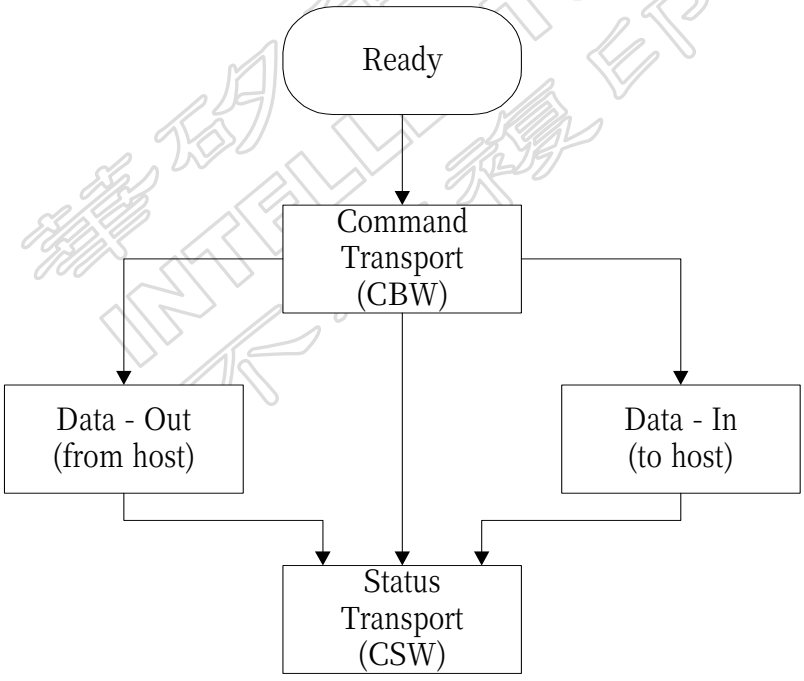
0: divided by 2 1: divided by 4
2: divided by 8 3: divided by 16
4: divided by 32 5: divided by 64
6: divided by 128 7: divided by 256
8: divided by 512 9: divided by 1024
10: divided by 2048 11: divided by 4096

5.12 USB CONTROLLER

MA8201-H72 USB controller implements the Bulk Only Transport protocols. Two endpoints Bulk-In and Bulk-Out are established in the USB bus initializing phase. Command, data and status are transferred via these two pipes connected with 64 bytes FIFO in the controller. The figure below shows the flow for Command Transfer, Data-In, Data-Out and Status Transport. The host shall send CBW, which contains a command block, to the device via the Bulk-Out endpoints. The CBS shall start on a packet boundary and end as a short packet with exactly 31 (1Fh) bytes transferred. The device shall indicate a successful transport of a CBW by ACKing the CBW. If the host detects a STALL of Bulk-Out endpoint during command transport, the host shall respond with a Reset Recovery.

All data transport shall begin on a packet boundary. The host shall attempt to transfer the exact number of bytes to or from the device as specified by the dCBWDataTransferLength and the Direction bit in the CBW. To report an error before data transport completes and to maximize data integrity, the device may terminate the command by stalling the endpoint in use (the Bulk-In endpoint during data in, the Bulk-Out endpoint during data out).

The device shall send each CSW to the host via the Bulk-In endpoint. The CSW shall start on a packet boundary and end ads a short packet with exactly 13(Dh) bytes transferred. The CSW indicates to the host the status of the execution of the command block form the correspond CWB. The dCSWDataResidue field indicates how much of the data transferred is to be considered processed or relevant. The host shall ignore any data received beyond that which is relevant.



Command/Data/Status Flow

Address	Bit	Name	Function	1	0	SR	R/W
0x1890 USB	D7	USBSHK	USB handshake status	ACK	NACK	0	R
	D6	BFFUL	Buffer full	Full	Not Full	0	R
	D5	BFEMP	Buffer empty	Empty	Not Empty	1	R
	D4	MS_RST	Mass Storage Reset	Reset (R)	Clear (R/W)	0	R/W
	D3	BOTEN	Enable BOT protocol	Enable	Disable	0	R/W
	D2	FCSW	Force into CSW	Enable	Disable	0	R/W
	D1	STALL	USB pipe stall	1	0	0	R/W
	D0	USB_GO	USB ready to go	Start	None	0	R/W

D7 : USB handshake status. 1 : ACK, 0 : NACK.

D6 : USB R/W buffer (0x1893) full. 1 : Full, 0 : Not full.

D5 : USB R/W buffer (0x1893) empty. 1 : Empty, 0 : Not empty.

D4 : Mass Storage Reset. Read : 1 : Host reset via class-specified request. 0 : none.
Write 1 to clear this bit.

D3 : Enable BOT protocol. 1 : USB controller takes care the Bulk Only Transport protocol and controls the flow automatically. 0 : Flow controlled by firmware.

D2 : Force into CSW. 1 : Force the transport phase into CSW. 0 : Disable

D1 : USB pipe stall. 1 : Stall the endpoint in use. 0 : Stall cancelled.

D0 : USB ready to go. 1 : Start the transfer. 0 : none.

Address	Bit	Name	Function	1		0		SR	R/W
0x1891 USB	D7	FCBW	interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D6	FDIN	interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D5	FDOUT	interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D4	FCSW	interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D3	ECBW	interrupt mask register	Enable		Mask		0	R/W
	D2	EDIN	interrupt mask register	Enable		Mask		0	R/W
	D1	EDOUT	interrupt mask register	Enable		Mask		0	R/W
	D0	ECSW	interrupt mask register	Enable		Mask		0	R/W

D7: CBW interrupt flag. Used only in BOT mode. 1 : A CBW packet received. 0 : none. Write 1 to clear this bit.

D6 : Data-In interrupt flag. It indicates two different meanings in BOT and none-BOT mode.
In BOT mode : 1 : A packet transfer in BOT Data-In phase finished. 0 : none. Write 1 to clear this bit.
In non-BOT mode : 1 : A Bulk-In packet transfer finished. 0 : none. Write 1 to clear this bit.

D5 : CSW interrupt flag. Used only in BOT mode. 1 : A CSW packet transmitted. 0 : none. Write 1 to clear this bit.

D4 : Data-Out interrupt flag. It indicates two different meanings in BOT an d none-BOT mode.

In BOT mode : 1 : A packet transfer in BOT Data-Out phase finished. 0 : none. Write 1 to clear this bit.

In non-BOT mode : 1 : A Bulk-Out packet transfer finished. 0 : none. Write 1 to clear this bit.

D3 : CBW interrupt mask. 1 : Enable interrupt, 0 : mask.

D2 : Data-In interrupt mask. 1 : Enable interrupt, 0 : mask.

D1 : Data-Out interrupt mask. 1 : Enable interrupt, 0 : mask.

D0 : CSW interrupt mask. 1 : Enable interrupt, 0 : mask.

Address	Bit	Name	Function	1	0	SR	R/W
0x1892 USB	D7	MLUM3	Maximum Logical Unit Number	High	Low	0	R/W
	D6	MLUN2		High	Low		
	D5	MLUN1		High	Low		
	D4	MLUN0		High	Low		
	D3	SUSEN	USB suspend enable	Enable	Disable	0	R/W
	D2	BTIPORT	Block Transfer Port	Enable	Disable	0	R/W
	D1	WBPRST	Write Buffer pointer reset	Reset	None	0	W
	D0	RBPRST	Read Buffer pointer reset	Reset	None	0	W

D7 ~ D4 : Maximum Logical Unit Number.

D3 : USB suspend enable. 1 : Enable suspend function, 0 : Disable.

D2 : Block Transfer Port. 1 : Data transfer by direct hardware access. 0 : Data transfer by CPU access.

D1 : Write Buffer pointer reset. 1 : Reset write buffer point. 0 : none.

D0 : Read Buffer pointer reset. 1 : Reset read buffer point. 0 : none.

Address	Bit	Name	Function	1	0	SR	R/W
0x1893 USB	D7	USBD7	USB R/W Buffer (Buffer Length =64 Bytes)	High	Low	0	R/W
	D6	USBD6		High	Low	0	R/W
	D5	USBD5		High	Low	0	R/W
	D4	USBD4		High	Low	0	R/W
	D3	USBD3		High	Low	0	R/W
	D2	USBD2		High	Low	0	R/W
	D1	USBD1		High	Low	0	R/W
	D0	USBD0		High	Low	0	R/W

D7 ~ D0 :USB R/W buffer.

Address	Bit	Name	Function	1	0	SR	R/W
0x1894 USB	D7	USBVID7	Vender ID Bit 7 ~ 0	High	Low	0	R/W
	D6	USBVID6		High	Low	0	R/W
	D5	USBVID5		High	Low	1	R/W
	D4	USBVID4		High	Low	0	R/W
	D3	USBVID3		High	Low	1	R/W
	D2	USBVID2		High	Low	0	R/W
	D1	USBVID1		High	Low	1	R/W
	D0	USBVID0		High	Low	0	R/W
0x1895 USB	D7	USBVID15	Vender ID Bit 15 ~ 8	High	Low	0	R/W
	D6	USBVID14		High	Low	0	R/W
	D5	USBVID13		High	Low	0	R/W
	D4	USBVID12		High	Low	0	R/W
	D3	USBVID11		High	Low	0	R/W
	D2	USBVID10		High	Low	1	R/W
	D1	USBVID9		High	Low	1	R/W
	D0	USBVID8		High	Low	0	R/W
0x1896 USB	D7	MAXCUR7	Maximum Current Bit 7 ~ 0 (in unit of 2 mA)	High	Low	0	R/W
	D6	MAXCUR6		High	Low	0	R/W
	D5	MAXCUR5		High	Low	1	R/W
	D4	MAXCUR4		High	Low	1	R/W
	D3	MAXCUR3		High	Low	0	R/W
	D2	MAXCUR2		High	Low	0	R/W
	D1	MAXCUR1		High	Low	1	R/W
	D0	MAXCUR0		High	Low	0	R/W
0x1898 USB	D7	SNUM0_7	Serial Number Byte 0	High	Low	0	R/W
	D6	SNUM0_6		High	Low	0	R/W
	D5	SNUM0_5		High	Low	1	R/W
	D4	SNUM0_4		High	Low	1	R/W
	D3	SNUM0_3		High	Low	0	R/W
	D2	SNUM0_2		High	Low	0	R/W
	D1	SNUM0_1		High	Low	0	R/W
	D0	SNUM0_0		High	Low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x1899 USB	D7	SNUM1_7	Serial Number Byte 1	High	Low	0	R/W
	D6	SNUM1_6		High	Low	0	R/W
	D5	SNUM1_5		High	Low	1	R/W
	D4	SNUM1_4		High	Low	1	R/W
	D3	SNUM1_3		High	Low	0	R/W
	D2	SNUM1_2		High	Low	0	R/W
	D1	SNUM1_1		High	Low	0	R/W
	D0	SNUM1_0		High	Low	1	R/W
0x189A USB	D7	SNUM2_7	Serial Number Byte 2	High	Low	0	R/W
	D6	SNUM2_6		High	Low	1	R/W
	D5	SNUM2_5		High	Low	0	R/W
	D4	SNUM2_4		High	Low	0	R/W
	D3	SNUM2_3		High	Low	0	R/W
	D2	SNUM2_2		High	Low	0	R/W
	D1	SNUM2_1		High	Low	0	R/W
	D0	SNUM2_0		High	Low	1	R/W
0x189B USB	D7	SNUM3_7	Serial Number Byte 3	High	Low	0	R/W
	D6	SNUM3_6		High	Low	1	R/W
	D5	SNUM3_5		High	Low	0	R/W
	D4	SNUM3_4		High	Low	0	R/W
	D3	SNUM3_3		High	Low	0	R/W
	D2	SNUM3_2		High	Low	0	R/W
	D1	SNUM3_1		High	Low	0	R/W
	D0	SNUM3_0		High	Low	1	R/W

0x1894 ~ 0x189B : Define the Vender ID, maximum current and serial number.

Address	Bit	Name	Function	1	0	SR	R/W
0x189C USB	D7	DITL_7	Data In Transfer Length	High	Low	0	R/W
	D6	DITL_6		High	Low	1	R/W
	D5	DITL_5		High	Low	0	R/W
	D4	DITL_4		High	Low	0	R/W
	D3	DITL_3		High	Low	0	R/W
	D2	DITL_2		High	Low	0	R/W
	D1	DITL_1		High	Low	0	R/W
	D0	DITL_0		High	Low	0	R/W

D7 ~ D0 : Expected Data In Transfer Length.

Address	Bit	Name	Function	1	0	SR	R/W
0x189D USB	D7	DIUTL_7	Data In USB Transfer Length	High	Low	0	R
	D6	DIUTL_6		High	Low	0	R
	D5	DIUTL_5		High	Low	0	R
	D4	DIUTL_4		High	Low	0	R
	D3	DIUTL_3		High	Low	0	R
	D2	DIUTL_2		High	Low	0	R
	D1	DIUTL_1		High	Low	0	R
	D0	DIUTL_0		High	Low	0	R

D7 ~ D0 : The actual transfer length of Data-In.

Address	Bit	Name	Function	1	0	SR	R/W
0x189E USB	D7	DOTL_7	Data Out Transfer Length	High	Low	0	R/W
	D6	DOTL_6		High	Low	1	R/W
	D5	DOTL_5		High	Low	0	R/W
	D4	DOTL_4		High	Low	0	R/W
	D3	DOTL_3		High	Low	0	R/W
	D2	DOTL_2		High	Low	0	R/W
	D1	DOTL_1		High	Low	0	R/W
	D0	DOTL_0		High	Low	0	R/W

D7 ~ D0 : Expected Data Out Transfer Length.

Address	Bit	Name	Function	1	0	SR	R/W
0x189F USB	D7	DOUTL_7	Data Out USB Transfer Length	High	Low	0	R
	D6	DOUTL_6		High	Low	0	R
	D5	DOUTL_5		High	Low	0	R
	D4	DOUTL_4		High	Low	0	R
	D3	DOUTL_3		High	Low	0	R
	D2	DOUTL_2		High	Low	0	R
	D1	DOUTL_1		High	Low	0	R
	D0	DOUTL_0		High	Low	0	R

D7 ~ D0 : The actual transfer length of Data-Out.

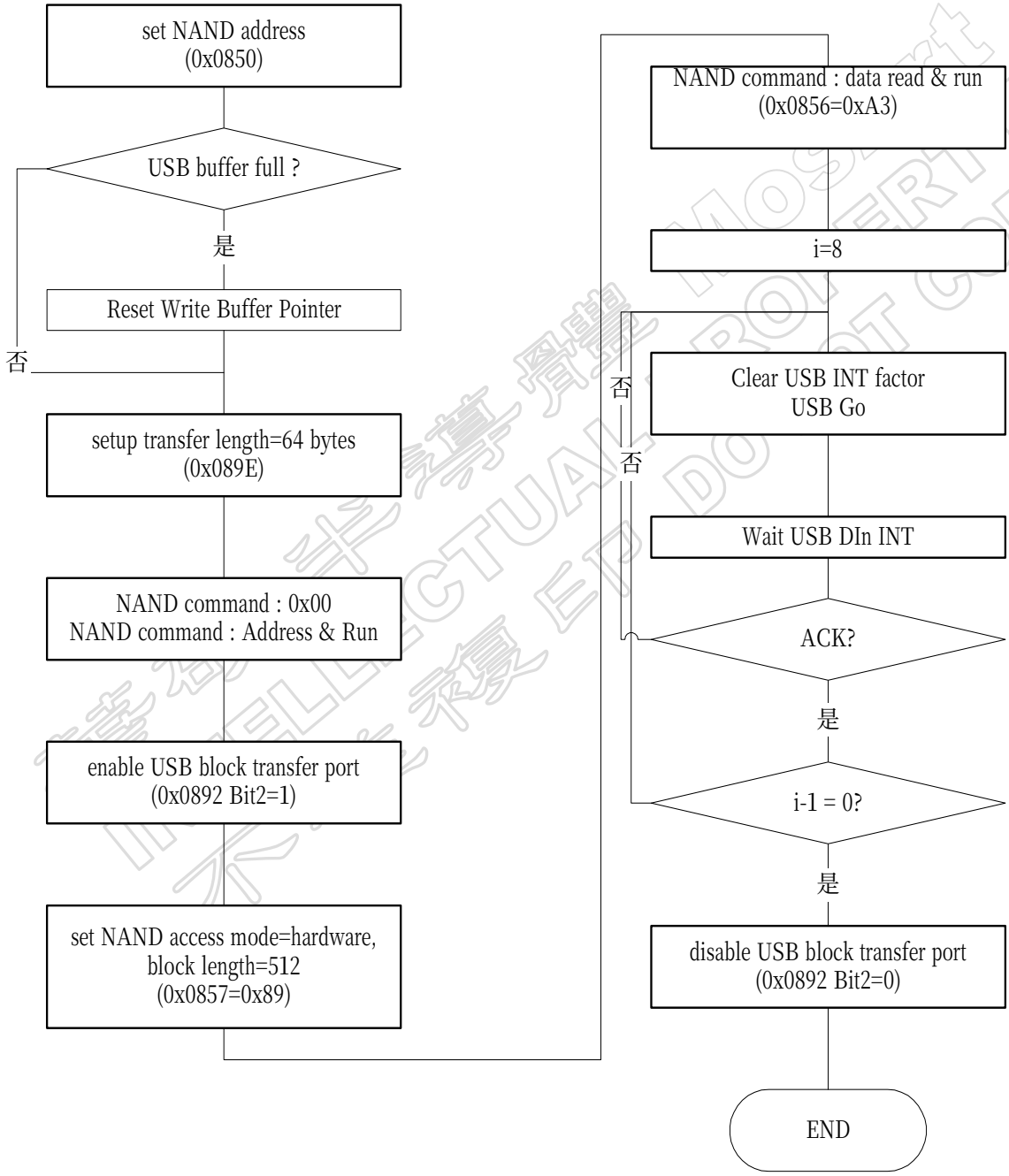
Address	Bit	Name	Function	1	0	SR	R/W
0x1870 USB	D7	USBPID7	Product ID Bit 7 ~ 0	High	Low	0	R/W
	D6	USBPID6		High	Low	0	R/W
	D5	USBPID5		High	Low	0	R/W
	D4	USBPID4		High	Low	1	R/W
	D3	USBPID3		High	Low	1	R/W
	D2	USBPID2		High	Low	0	R/W
	D1	USBPID1		High	Low	0	R/W
	D0	USBPID0		High	Low	0	R/W
0x1871 USB	D7	USBVPD15	Product ID Bit 15 ~ 8	High	Low	0	R/W
	D6	USBVPD14		High	Low	1	R/W
	D5	USBVPD13		High	Low	1	R/W
	D4	USBVPD12		High	Low	0	R/W
	D3	USBVPD11		High	Low	0	R/W
	D2	USBVPD10		High	Low	1	R/W
	D1	USBPID9		High	Low	1	R/W
	D0	USBPID8		High	Low	0	R/W

0x1870 ~ 0x1871 : Define the Product ID.

5.12.1 PROGRAM FLOW

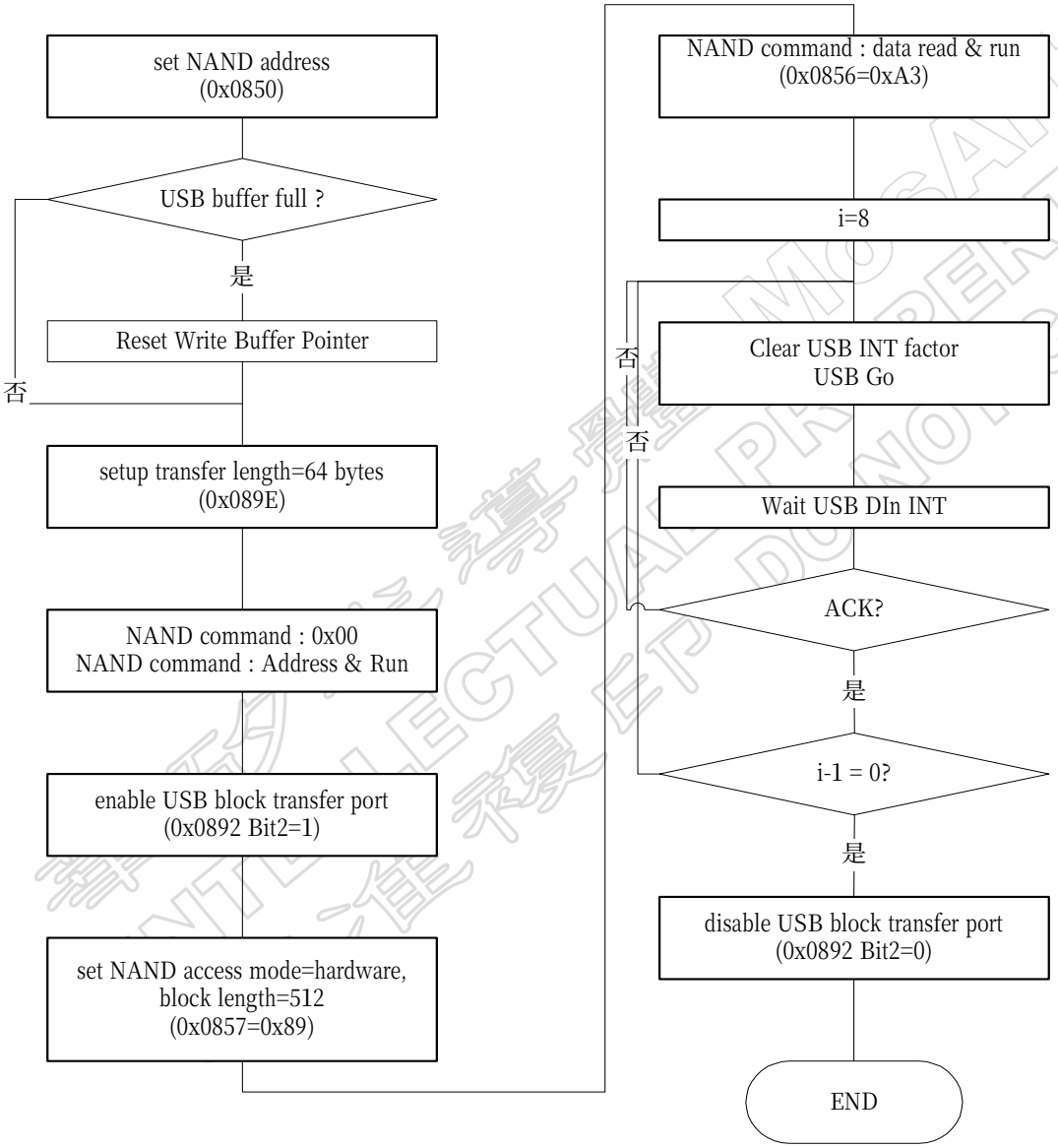
Read Flow Chat

NAND -> USB Pipe



Write Flow Chart

NAND -> USB Pipe



5.12.2 EXAMPLES OF PROGRAM

```
/*********************************************************************/
/*      read pages(512 bytes) from NAND to USB pipe     */
/*  input:                                              */
/*      wPageCtr=number of NAND pages have to read  */
/*      *((volatile Dword *)(0x1850))=NAND address      */
/*  return:                                             */
/*      __TRUE      command success                     */
/*      __FALSE     command fail                        */
/*********************************************************************/

#define _NAND_CMD(bCmd) {   _SFR0854=bCmd;      \
                            _SFR0855=_00111000b; \
                            _SFR0856=_10100000b; \
                            while(!ubmSFR0855.sBit._3) {}   }   /* write command to NAND flash */
Byte bNAND2Pipe(Word wPageCtr)
{
    Byte    i, bReturnStatus, abNANDSpareAreaBuf[16];
    bReturnStatus=__TRUE;
    ubmSFR0856.sBit._7=1;                           /* enable NAND CE */
    ubmSFR0890.sBit._0=0;                           /* disable USB transfer */
    if (ubmSFR0890.sBit._6) {                       /* if USB buffer full, reset write buffer pointer */
        ubmSFR0892.sBit._1=1;                       /* reset USB write buffer pointer */
    }
    _SFR089C=64;                                    /* setup transfer length=64 bytes */
    for (; wPageCtr>0; --wPageCtr) {
        _NAND_CMD(0x00);                            /* write command "00" */
        _SFR0856=_10100001b;                        /* NAND command mode=address & run */
        while(!ubmSFR0855.sBit._4) {}               /* wait NAND BUSY status finished */
        _SFR0857=(_10000000b | __NAND_CLK_RATE | 9);    /* set NAND access mode=auto, data rate=clock/2 & block
length=512 */
        _SFR0858=_00100001b;                        /* set ECC mode=ODD, READ, START */
        _SFR0855=_00111000b;                        /* clear NAND IF */
        _SFR0856=_10100011b;                        /* NAND command mode=data read & run */
    /* USB direct transfer mode */
        ubmSFR0892.sBit._2=1;               /* enable USB transfer mode = NAND 2 USB direct data transfer mode */
        i=8;
        do {
            _SFR0891|=_11110000b;                   /* clear USB IF */
            ubmSFR0890.sBit._0=1;                   /* enable USB transfer */
            while(!ubmSFR0891.sBit._6) {};          /* wait USB DIN interrupt */
            if (ubmSFR0890.sBit._7) {               /* USB ACK ? */
                --i;
            }
        } while(i);
        _SFR0891|=_11110000b;                       /* clear USB IF */
        ubmSFR0892.sBit._2=0;                       /* disable USB block transfer mode */
    /* read sapre area data (ECC) */
        ubmSFR0858.sBit._0=0;                       /* stop ECC */
        _SFR0857=(_00000000b | __NAND_CLK_RATE | 4);    /* set access mode=manual, data rate=clock/2, data
length=16 bytes */
        _SFR0856=_10100011b;                        /* NAND command mode=data read & run */
        for (i=0; i<16; ++i) {
            abNANDSpareAreaBuf[i]=_SFR0854;
        }
        ++_SFR0850;                                 /* increment NAND address */
        nop_instruction();                          /* skip NAND Twb(200ns), delay 83*4=498ns@12Mhz */
        nop_instruction();
        nop_instruction();
        nop_instruction();
        nop_instruction();
        nop_instruction();
        while (!ubmSFR0813.sBit._3) {}              /* wait NAND R/B goes high */
    /* check ECC */
        if (bNANDCheckBlockVolid())                 /* block volid ? */
        if (*(abNANDSpareAreaBuf+13) == _SFR0859)   /* 0x000~0x0FF ECC check */
        if (*(abNANDSpareAreaBuf+14) == _SFR085A)
        if (*(abNANDSpareAreaBuf+15) == _SFR085B)
        if (*(abNANDSpareAreaBuf+8)  == _SFR085C)   /* 0x100~0x1FF ECC check */
        if (*(abNANDSpareAreaBuf+9)  == _SFR085D)
```

```
            if (*(abNANDSpareAreaBuf+10) == _SFR085E) {
                continue;
            }

        /* error recovery process here ! */
            continue;
        }
        _SFR0857=0;                                     /* disable NAND block transfer mode */
        ubmSFR0856.sBit._7=0;                           /* disable NAND CE */
        return (bReturnStatus);
}
```

```
/*****************************************************************************/
/*      send data to USB pipe                                                */
/*      input:                                                               */
/*            wDataCtr          length of data to be send                    */
/*            *pbData           pointer of data to be send                   */
/*      return:                                                              */
/*            __TRUE          command success                                */
/*            __FALSE         command fail                                   */
/*****************************************************************************/

Byte bDevice2Host(Word wDataCtr, Byte *pbData)
{
    Byte    i, bTxLengthTemp, bReturnStatus;
    bReturnStatus=__TRUE;
    if (ubmSFR0890.sBit._6) {                       /* if buffer full, reset write buffer pointer */
        ubmSFR0892.sBit._1=1;                       /* reset USB write buffer pointer */
    }
while (wDataCtr && bReturnStatus) {
        if (wDataCtr >= 64) {                       /* check trnasfer length */
            wDataCtr-=64;
            bTxLengthTemp=64;
        } else {
            bTxLengthTemp=(Byte)wDataCtr;
            wDataCtr=0;
        }
_SFR089C=i=bTxLengthTemp;                           /* setup transfer length */
        for (i=bTxLengthTemp; i>0; --i, ++pbData) {
            _SFR0893=*pbData;
        }
        if (bTxLengthTemp!=64) {                    /* reset USB write buffer pointer if data langth less than 64 */
            ubmSFR0892.sBit._1=1;
        }
for (;;) {
            _SFR0891|=_11110000b;                   /* clear USB IF */
            ubmSFR0890.sBit._0=1;                   /* enable USB transfer */
            while (!ubmSFR0891.sBit._6) {}          /* wait USB DIN interrupt */
            if (ubmSFR0890.sBit._7) {               /* USB ACK ? */
                break;
            }
        }
        _SFR0891|=_11110000b;                       /* clear USB IF */
        if (_SFR089D != bTxLengthTemp) {            /* check transfer length correct */
            bReturnStatus=__FALSE;                  /* transfer length error */
        }
    }
    return (bReturnStatus);
}
```

```
/*****************************************************************************/
/*      write data from USB pipe to specified NAND address   */
/*  input:                                                   */
/*      wPageCtr=number of NAND pages have to write          */
/*      *((volatile Dword *)(0x1850))=NAND address           */
/*  global:                                                  */
/*      wBlockAddFieldData=NAND block address                */
/*  return:                                                  */
/*      __TRUE      command success                          */
/*      __FALSE     command fail                             */
/*****************************************************************************/

#define _NAND_CMD(bCmd) {   _SFR0854=bCmd;      \
                            _SFR0855=_00111000b; \
                            _SFR0856=_10100000b; \
                            while(!ubmSFR0855.sBit._3) {}   }   /* write command to NAND flash */

Byte bPipe2NAND(Word wPageCtr)
{
    Byte    i, bReturnStatus;
    bReturnStatus=__TRUE;
    ubmSFR0856.sBit._7=1;                           /* enable NAND CE */
    ubmSFR0890.sBit._0=0;                           /* disable USB transfer */
    _SFR089E=64;                                    /* setup transfer length=64 bytes */
    for (; wPageCtr>0; --wPageCtr) {
        _SFR0858=_00100011b;                        /* set ECC mode=ODD, WRITE, START */
        _NAND_CMD(0x00);                            /* write command "00" */
        _NAND_CMD(0x80);                            /* write command "80" */
        _SFR0856=_10100001b;                        /* NAND command mode=address & run */
        while(!ubmSFR0855.sBit._3) {}               /* wait command finished */
        ubmSFR0892.sBit._2=1;           /* enable USB transfer mode = NAND 2 USB direct data transfer mode */
        _SFR0857=(_10000000b | __NAND_CLK_RATE | 9);    /* set NAND access mode=auto, data rate=clock/2 & block
length=512 */
        _SFR0855=_00111000b;                        /* clear NAND IF */
        _SFR0856=_10100010b;                        /* NAND command mode=data write & run */
        i=8;                                        /* transfer 512 bytes (64*8) */
        do {
            _SFR0891|=_11110000b;                   /* clear USB IF */
            ubmSFR0890.sBit._0=1;                   /* enable USB transfer */
            while(!ubmSFR0891.sBit._5) {};          /* wait USB DOUT interrupt */
            if (ubmSFR0890.sBit._7) {               /* USB ACK ? */
                --i;
            }
        } while (i);
        _SFR0891|=_11110000b;                       /* clear USB IF */
        while(!ubmSFR0855.sBit._3) {}               /* wait command finished */
        ubmSFR0892.sBit._2=0;                       /* disable direct data transfer mode */
        ubmSFR0858.sBit._0=0;                       /* stop ECC */
    /* write NAND spare area data */
        _SFR0857=(_00000000b | __NAND_CLK_RATE | 4);    /* set access mode=manual, data rate=clock/2, data
length=16 bytes */
        _SFR0856=_10100010b;                        /* NAND command mode=data write & run */
        _SFR0854=0xFF;
        _SFR0854=0xFF;
        _SFR0854=0xFF;
        _SFR0854=0xFF;
        _SFR0854=0xFF;                              /* data staus byte */
        _SFR0854=0xFF;                              /* block status byte */
        _SFR0854=*(((Byte*)(&wBlockAddFieldData))+1);   /* write block address */
        _SFR0854=(Byte)wBlockAddFieldData;
        _SFR0854=_SFR085C;                          /* 0x100~0x1FF ECC */
        _SFR0854=_SFR085D;
        _SFR0854=_SFR085E;
        _SFR0854=*(((Byte*)(&wBlockAddFieldData))+1);   /* write block address */
        _SFR0854=(Byte)wBlockAddFieldData;
        _SFR0854=_SFR0859;                          /* 0x000~0x0FF ECC */
        _SFR0854=_SFR085A;
        _SFR0854=_SFR085B;
        _NAND_CMD(0x10);                            /* write command "10" */
        while(!ubmSFR0855.sBit._4) {}               /* wait NAND BUSY status finished */
        _NAND_CMD(0x70);                            /* write command "70" */
        _SFR0857=(_00000000b | __NAND_CLK_RATE | 0);    /* set access mode=manual, data rate=clock/2, data
length=1 byte */
```

```
        _SFR0856=_10100011b;                    /* NAND command mode=data read & run */
        i=_SFR0854;                             /* read write status */
        if (i & _00000001b) {                   /* bit0=write status, 0=success, 1=fail */
            bNANDMarkBlockFail();               /* mark block fail */
            bReturnStatus=__FALSE;
            break;
        }
        ++*((volatile Dword *)(0x1850));        /* increment NAND address */
    }
    _SFR0857=0;                                 /* disable NAND block transfer mode */
    ubmSFR0892.sBit._2=0;                       /* disable USB block transfer mode */
    ubmSFR0856.sBit._7=0;                       /* disable NAND CE */
    return (bReturnStatus);
}
```

```
/*****************************************************************************/
/*      receive CBW form USB pipe                                            */
/*      input: void                                                          */
/*      global:                                                              */
/*          uCBW=CBW data buffer                                             */
/*      return:                                                              */
/*          __TRUE      command success                                      */
/*          __FALSE     command fail                                         */
/*****************************************************************************/
Byte bUSBRxCBW(void)
{
    Byte    i, bReturnStatus;
    bReturnStatus=__TRUE;
    for (;;) {
        _SFR0891|=_11110000b;                   /* clear USB IF */
        ubmSFR0890.sBit._0=1;                   /* start USB transfer */
        while (!ubmSFR0891.sBit._7) {};         /* wait CBW interrupt */
        if (!ubmSFR0890.sBit._7) {              /* USB handshake correct (ACK) ? */
            continue;
        }
        _SFR089E=sizeof(uCBW);                  /* setup transfer length */
        for (i=0; i<sizeof(uCBW); ++i) {
            if (ubmSFR0890.sBit._5) {           /* buffer empty ? */
                break;
            }
            uCBW.byte[i]=_SFR0893;
        }
        if (_SFR089F != sizeof(uCBW)) {         /* check transfer length correct */
            bReturnStatus=__FALSE;
            bUSBStallPipe();                    /* stall the pipe if length incorrect */
            break;
        }
        ubmSFR0892.sBit._0=1;                   /* reset USB read buffer pointer */
        break;
    }
    ubmSFR0890.sBit._0=1;                       /* start USB transfer */
    return (bReturnStatus);
}
```

```
/*****************************************************************************/
/*        stall USB transfer pipe                                            */
/*        input:   void                                                      */
/*        return:                                                            */
/*              __TRUE        command success                               */
/*              __FALSE       command fail                                  */
/*****************************************************************************/
Byte bUSBStallPipe(void)
{
    Byte      bReturnStatus;

    bReturnStatus=__TRUE;
    _SFR089C=0;                                         /* clear transfer length register */
    ubmSFR0892.sBit._1=1;                               /* reset USB write buffer pointer */
    _SFR0890=_00001010b;                                /* set stall flag, clear reset status */
    Timer1Start(_Timer1msMode, __TIME_BULKTRANSFER_TIMEOUT);      /* start timer */
    for (;;) {
        Timer1CheckStatus();                            /* Timer1 loop */
        if (_SFR0890 & _00010000b) {                    /* Mess storage reset ? */
            break;
        }
        if (fTimer1ms) {                                /* transfer time-out ? */
            bReturnStatus=__FALSE;
            break;
        }
        if (_SFR0891 & _11110000b) {                    /* get any interrupt ? */
            break;
        }
    }
    Timer1Stop();
    _SFR0891 |= _11110000b;                             /* clear USB IF */
    _SFR0890=_00001000b;                                /* clear stall & USB reset flag */
    ubmSFR0892.sBit._0=1;                               /* reset USB read buffer pointer to make FIFO data volid */
    return (bReturnStatus);
}
```

5.13 32/16 UNSINGED DIVIDER

The divider can process 32 bits dividend and 16 bits divisor. Then it produces 16 quotient bits and 16 remainder bits by taking 17 system clocks. Because the quotient is 16 bits, be sure that the upper 16 bits of dividend must be less than the divisor.

Address	Bit	Name	Function	1	0	SR	R/W
0x18A0 Divide Register	D7	DIVID7	Dividend data 7/ Quotient 7	High	Low	0	R/W
	D6	DIVID6	Dividend data 6/ Quotient 6	High	Low	0	R/W
	D5	DIVID5	Dividend data 5/ Quotient 5	High	Low	0	R/W
	D4	DIVID4	Dividend data 4/ Quotient 4	High	Low	0	R/W
	D3	DIVID3	Dividend data 3/ Quotient 3	High	Low	0	R/W
	D2	DIVID2	Dividend data 2/ Quotient 2	High	Low	0	R/W
	D1	DIVID1	Dividend data 1/ Quotient 1	High	Low	0	R/W
	D0	DIVID0	Dividend data 0/ Quotient 0	High	Low	0	R/W
0x18A1 Divide Register	D7	DIVID15	Dividend data 15/ Quotient 15	High	Low	0	R/W
	D6	DIVID14	Dividend data 14/ Quotient 14	High	Low	0	R/W
	D5	DIVID13	Dividend data 13/ Quotient 13	High	Low	0	R/W
	D4	DIVID12	Dividend data 12/ Quotient 12	High	Low	0	R/W
	D3	DIVID11	Dividend data 11/ Quotient 11	High	Low	0	R/W
	D2	DIVID10	Dividend data 10/ Quotient 10	High	Low	0	R/W
	D1	DIVID9	Dividend data 9/ Quotient 9	High	Low	0	R/W
	D0	DIVID8	Dividend data 8/ Quotient 8	High	Low	0	R/W
0x18A2 Divide Register	D7	DIVID23	Dividend data 23/ Remainder 15	High	Low	0	R/W
	D6	DIVID22	Dividend data 22/ Remainder 14	High	Low	0	R/W
	D5	DIVID21	Dividend data 21/ Remainder 13	High	Low	0	R/W
	D4	DIVID20	Dividend data 20/ Remainder 12	High	Low	0	R/W
	D3	DIVID19	Dividend data 19/ Remainder 11	High	Low	0	R/W
	D2	DIVID18	Dividend data 18/ Remainder 10	High	Low	0	R/W
	D1	DIVID17	Dividend data 17/ Remainder 9	High	Low	0	R/W
	D0	DIVID16	Dividend data 16/ Remainder 8	High	Low	0	R/W
0x18A3 Divide Register	D7	DIVID31	Dividend data 31/ Remainder 7	High	Low	0	R/W
	D6	DIVID30	Dividend data 30/ Remainder 6	High	Low	0	R/W
	D5	DIVID29	Dividend data 29/ Remainder 5	High	Low	0	R/W
	D4	DIVID28	Dividend data 28/ Remainder 4	High	Low	0	R/W
	D3	DIVID27	Dividend data 27/ Remainder 3	High	Low	0	R/W
	D2	DIVID26	Dividend data 26/ Remainder 2	High	Low	0	R/W
	D1	DIVID25	Dividend data 25/ Remainder 1	High	Low	0	R/W
	D0	DIVID24	Dividend data 24/ Remainder 0	High	Low	0	R/W

0x8A0 ~ 0x8A3 : Write : Dividend, Read : Quotient and Remainder

Address	Bit	Name	Function	1	0	SR	R/W
0x18A4 Divide Register	D7	DIVIS7	Divisor data 7	High	Low	0	W
	D6	DIVID6	Divisor data 6	High	Low	0	W
	D5	DIVID5	Divisor data 5	High	Low	0	W
	D4	DIVID4	Divisor data 4	High	Low	0	W
	D3	DIVID3	Divisor data 3	High	Low	0	W
	D2	DIVID2	Divisor data 2	High	Low	0	W
	D1	DIVID1	Divisor data 1	High	Low	0	W
	D0	DIVID0	Divisor data 0	High	Low	0	W
0x18A5 Divide Register	D7	DIVID15	Divisor data 15	High	Low	0	W
	D6	DIVID14	Divisor data 14	High	Low	0	W
	D5	DIVID13	Divisor data 13	High	Low	0	W
	D4	DIVID12	Divisor data 12	High	Low	0	W
	D3	DIVID11	Divisor data 11	High	Low	0	W
	D2	DIVID10	Divisor data 10	High	Low	0	W
	D1	DIVID9	Divisor data 9	High	Low	0	W
	D0	DIVID8	Divisor data 8	High	Low	0	W

0x8A4 ~ 0x8A5 : divisor

Address	Bit	Name	Function	1		0		SR	R/W
0x18A6 Divide Register	D7								
	D6								
	D5								
	D4								
	D3								
	D2								
	D1	DFF	Divider finish flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D0								

D1 : finish flag, read 0 = processing, read 1 = operation finished, write 1 = clear flag, write 0 = none

An action writing to address 0x8A5 will trigger division. After 17 system clocks, the finish flag asserts and indicates process is finished. Be sure that the higher byte of divisor MUST be the last byte to program. It means that programmers must write dividend and the lower byte of divisor firstly, then the higher byte of divisor.

5.14 16x16 UNSINGED MULTIPLICATION

The MA8201-H72 has a 16X16 unsigned multiplication to increase core CPU arithmetical performance.

Address	Bit	Name	Function	1	0	SR	R/W
0x18A8 Multiply Register	D7	MCAND7	Multiplicand data 7/ Product 7	High	Low	0	R/W
	D6	MCAND6	Multiplicand data 6/ Product 6	High	Low	0	R/W
	D5	MCAND5	Multiplicand data 5/ Product 5	High	Low	0	R/W
	D4	MCAND4	Multiplicand data 4/ Product 4	High	Low	0	R/W
	D3	MCAND3	Multiplicand data 3/ Product 3	High	Low	0	R/W
	D2	MCAND2	Multiplicand data 2/ Product 2	High	Low	0	R/W
	D1	MCAND1	Multiplicand data 1/ Product 1	High	Low	0	R/W
	D0	MCAND0	Multiplicand data 0/ Product 0	High	Low	0	R/W
0x18A9 Multiply Register	D7	MCAND15	Multiplicand data 15/ Product 15	High	Low	0	R/W
	D6	MCAND14	Multiplicand data 14/ Product 14	High	Low	0	R/W
	D5	MCAND13	Multiplicand data 13/ Product 13	High	Low	0	R/W
	D4	MCAND12	Multiplicand data 12/ Product 12	High	Low	0	R/W
	D3	MCAND11	Multiplicand data 11/ Product 11	High	Low	0	R/W
	D2	MCAND10	Multiplicand data 10/ Product 10	High	Low	0	R/W
	D1	MCAND9	Multiplicand data 9/ Product 9	High	Low	0	R/W
	D0	MCAND8	Multiplicand data 8/ Product 8	High	Low	0	R/W

CPU Write : Multiplicand data bit [15:0]

CPU Read : Multiplication result data bit [15:0]

Address	Bit	Name	Function	1	0	SR	R/W
0x18AA Multiply Register	D7	MIER7	Multiplier data 7/ Product 23	High	Low	0	R/W
	D6	MIER6	Multiplier data 6/ Product 22	High	Low	0	R/W
	D5	MIER5	Multiplier data 5/ Product 21	High	Low	0	R/W
	D4	MIER4	Multiplier data 4/ Product 20	High	Low	0	R/W
	D3	MIER3	Multiplier data 3/ Product 19	High	Low	0	R/W
	D2	MIER2	Multiplier data 2/ Product 18	High	Low	0	R/W
	D1	MIER1	Multiplier data 1/ Product 17	High	Low	0	R/W
	D0	MIER0	Multiplier data 0/ Product 16	High	Low	0	R/W
0x18AB Multiply Register	D7	MIER15	Multiplier data 15/ Product 31	High	Low	0	R/W
	D6	MIER14	Multiplier data 14/ Product 30	High	Low	0	R/W
	D5	MIER13	Multiplier data 13/ Product 29	High	Low	0	R/W
	D4	MIER12	Multiplier data 12/ Product 28	High	Low	0	R/W
	D3	MIER11	Multiplier data 11/ Product 27	High	Low	0	R/W
	D2	MIER10	Multiplier data 10/ Product 26	High	Low	0	R/W
	D1	MIER9	Multiplier data 9/ Product 25	High	Low	0	R/W
	D0	MIER8	Multiplier data 8/ Product 24	High	Low	0	R/W

CPU Write : Multiplier data bit [15:0]

CPU Read : Multiplication result data bit [31:16]

Address	Bit	Name	Function	1		0		SR	R/W
0x18AC Multiply Register	D7								
	D6								
	D5								
	D4								
	D3								
	D2								
	D1	MULTF	Multiplication finish flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D0								

D1 : finish flag, read 0 = processing, read 1 = operation finished, write 1 = clear flag, write 0 = none

An action writing to address 0x8AB will trigger multiplication. After about 16 CPU clocks, the finish flag asserts and indicates process is finished. Be sure that the higher byte of multiplier MUST be the last byte to program. It means that programmers must write multiplicand and the lower byte of multiplier firstly, then the higher byte of multiplier.

5.15 DATA REARRANGEMENT REGISTERS

Address	Bit	Name	Function	1	0	SR	R/W
0x18B0 DR Register	D7	DRD7	DR Write Data 7/ DR Read Data 31	High	Low	0	R/W
	D6	DRD6	DR Write Data 6/ DR Read Data 30	High	Low	0	R/W
	D5	DRD5	DR Write Data 5/ DR Read Data 29	High	Low	0	R/W
	D4	DRD4	DR Write Data 4/ DR Read Data 28	High	Low	0	R/W
	D3	DRD3	DR Write Data 3/ DR Read Data 27	High	Low	0	R/W
	D2	DRD2	DR Write Data 2/ DR Read Data 26	High	Low	0	R/W
	D1	DRD1	DR Write Data 1/ DR Read Data 25	High	Low	0	R/W
	D0	DRD0	DR Write Data 0/ DR Read Data 24	High	Low	0	R/W
0x18B1 DR Register	D7	DRD15	DR Write Data 15/ DR Read Data 23	High	Low	0	R/W
	D6	DRD14	DR Write Data 14/ DR Read Data 22	High	Low	0	R/W
	D5	DRD13	DR Write Data 13/ DR Read Data 21	High	Low	0	R/W
	D4	DRD12	DR Write Data 12/ DR Read Data 20	High	Low	0	R/W
	D3	DRD11	DR Write Data 11/ DR Read Data 19	High	Low	0	R/W
	D2	DRD10	DR Write Data 10/ DR Read Data 18	High	Low	0	R/W
	D1	DRD9	DR Write Data 9/ DR Read Data 17	High	Low	0	R/W
	D0	DRD8	DR Write Data 8/ DR Read Data 16	High	Low	0	R/W
0x18B2 DR Register	D7	DRD23	DR Write Data 23/ DR Read Data 15	High	Low	0	R/W
	D6	DRD22	DR Write Data 22/ DR Read Data 14	High	Low	0	R/W
	D5	DRD21	DR Write Data 21/ DR Read Data 13	High	Low	0	R/W
	D4	DRD20	DR Write Data 20/ DR Read Data 12	High	Low	0	R/W
	D3	DRD19	DR Write Data 19/ DR Read Data 11	High	Low	0	R/W
	D2	DRD18	DR Write Data 18/ DR Read Data 10	High	Low	0	R/W
	D1	DRD17	DR Write Data 17/ DR Read Data 9	High	Low	0	R/W
	D0	DRD16	DR Write Data 16/ DR Read Data 8	High	Low	0	R/W
0x18B3 DR Register	D7	DRD31	DR Write Data 31/ DR Read Data 7	High	Low	0	R/W
	D6	DRD30	DR Write Data 30/ DR Read Data 6	High	Low	0	R/W
	D5	DRD29	DR Write Data 29/ DR Read Data 5	High	Low	0	R/W
	D4	DRD28	DR Write Data 28/ DR Read Data 4	High	Low	0	R/W
	D3	DRD27	DR Write Data 27/ DR Read Data 3	High	Low	0	R/W
	D2	DRD26	DR Write Data 26/ DR Read Data 2	High	Low	0	R/W
	D1	DRD25	DR Write Data 25/ DR Read Data 1	High	Low	0	R/W
	D0	DRD24	DR Write Data 24/ DR Read Data 0	High	Low	0	R/W

The Data written to 0x8A0 can be read from 0x8A3

The Data written to 0x8A1 can be read from 0x8A2

The Data written to 0x8A2 can be read from 0x8A1

The Data written to 0x8A3 can be read from 0x8A0

5.16 PARITY CHECK REGISTERS

Address	Bit	Name	Function	1	0	SR	R/W
0x18B4 MIS	D7	PCD7	Parity Check Data7	High	Low	0	W
	D6	PCD6	Parity Check Data6	High	Low	0	W
	D5	PCD5	Parity Check Data5	High	Low	0	W
	D4	PCD4	Parity Check Data4	High	Low	0	W
	D3	PCD3	Parity Check Data3	High	Low	0	W
	D2	PCD2	Parity Check Data2	High	Low	0	W
	D1	PCD1	Parity Check Data1	High	Low	0	W
	D0	PCD0	Parity Check Data0	High	Low	0	W

D7 ~ D0 : Parity Check Data

Address	Bit	Name	Function	1	0	SR	R/W
0x18B5 MIS	D2						
	D1						
	D0	PCB	Parity Check Bit	High	Low	0	R/W

D0 : Even Parity check result. Read : Parity Check bit. Write : 1 for odd parity check, 0 for even parity check.

5.17 DMA CONTROLLER

Address	Bit	Name	Function	1		0		SR	R/W
0x18C0 DMA Register	D3								
	D2	DMAEN	DMA enable	Enable		Disable		0	R/W
	D1	DMADIR	DMA direction	Ram to Flash		Flash to Ram		0	R/W
	D0	DMAGO	DMA start trigger	R	Busy	R	Ready	0	R/W
				W	Trigger	W	None		

D2 : enable DMA controller, 1: enable, 0: disable

D1 : DMA data stream direction, 0: load flash card data to ram, 1: load ram data to flash card

D0 : Read 1 : DMA busy, 0: idle

Write 1: DMA start trigger, 0: none

Address	Bit	Name	Function	1		0		SR	R/W
0x18C1 DMA Register	D2								
	D1	IDMA	DMA finish interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D0	EIDMA	DMA interrupt mask register	Enable		Mask		0	R/W

D1 : DMA interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D0 : DMA interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

Address	Bit	Name	Function	1	0	SR	R/W
0x18C2 DMA Register	D7	DMAA[7]	The RAM Start Address for DMA	DMAA[12:0] = 0x0000-17FF		00	R/W
	D6	DMAA[6]					
	D5	DMAA[5]					
	D4	DMAA[4]					
	D3	DMAA[3]					
	D2	DMAA[2]					
	D1	DMAA[1]					
	D0	DMAA[0]					
0x18C3 DMA Register	D4	DMAA[12]	The RAM Start Address for DMA	DMAA[12:0] = 0x0000-17FF		00	R/W
	D3	DMAA[11]					
	D2	DMAA[10]					
	D1	DMAA[9]					
	D0	DMAA[8]					

DMA[12:0] : The start address of RAM for DMA transfer (0x0000-17fff)

5.18 USB DMA CONTROLLER

Address	Bit	Name	Function	1		0		SR	R/W
0x18D0 USBDMA Register	D3	RUDMAEN	Ram and USBDMA data transfer enable	Enable		Disable		0	R/W
	D2								
	D1	DMAEN	DMA enable	Enable		Disable		0	R/W
	D0	DMAGO	DMA start trigger	R	Busy	R	Ready	0	R/W
				W	Trigger	W	None		

D1 : enable USB DMA controller, 1: enable, 0: disable

D0 : Read 1 : USB DMA busy, 0: idle

Write 1: USB DMA start trigger, 0: none

Address	Bit	Name	Function	1		0		SR	R/W
0x18D1 USBDMA Register	D5	IRRUDMA	Ram & USBDMA transfer finish interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D4	EIRRUDMA	Ram & USBDMA transfer interrupt mask register	Enable		Mask		0	R/W
	D3	IRDMA	Read DMA finish interrupt factor flag	R	Yes			0	R/W
				W	Reset	W	None		
	D2	EIRDMA	Read DMA interrupt mask register	Enable		Mask		0	R/W
	D1	IWDMA	Write DMA finish interrupt factor flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D0	EIWDMA	Write DMA interrupt mask register	Enable		Mask		0	R/W

D3 : USB read DMA interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D2 : USB read DMA interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

D1 : USB write DMA interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D0 : USB write DMA interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

Address	Bit	Name	Function	1	0	SR	R/W
0x18D2 USBDMA Register	D4						
	D3	DMABL[3]	USBDMA block length	Block Length = 2^BKL BKL = 0 ~ 9 (maximum 512 bytes)		00	R/W
	D2	DMABL[2]					
	D1	DMABL[1]					
	D0	DMABL[0]					

D[3:0] : USB DMA read/write block Length = 2^BKL BKL ranges in 0 ~ 9 (maximum 512 bytes)

Address	Bit	Name	Function	1		0		SR	R/W
0x18D3 USBDMA Register	D2								
	D1	RAMTEST	Start USBDMA SRAM BIST testing	R	Busy	R	Ready	0	R/W
				W	Trigger	W	None		
	D0	RAMPASS	SRAM BIST testing result	Pass		No pass		1	R

D1 : Read 1 : SRAM BIST testing busy, 0: ready

Write 1: SRAM BIST testing start to test, 0: none

D0 : USB DMA SRAM testing result, 1: pass, 0: no pass

Address	Bit	Name	Function	1	0	SR	R/W
0x18D4 USBDMA Register	D4						
	D3	RAM0S[1]	DMA SRAM 0 status	00 : empty ; 01 : full 10 : read busy 11 : write busy		0	R
	D2	RAM0S[0]					
	D1	RAM1S[1]	DMA SRAM 1 status	00 : empty ; 01 : full 10 : read busy 11 : write busy		0	R
	D0	RAM1S[0]					

D[3:2] : USB DMA SRAM block 0 status, 00 : empty, 01 : full, 10 : read busy, 11 : write busy

D[1:0] : USB DMA SRAM block 1 status, 00 : empty, 01 : full, 10 : read busy, 11 : write busy

Address	Bit	Name	Function	1	0	SR	R/W
0x18D5 USBDMA Register	D7	RAMAD [7]	Address for CPU read or write RAM of USBDMA	High	Low	0	R/W
	D6	RAMAD [6]					
	D5	RAMAD [5]					
	D4	RAMAD [4]					
	D3	RAMAD [3]					
	D2	RAMAD [2]					
	D1	RAMAD [1]					
	D0	RAMAD [0]					

D[7:0] : Address for CPU read or write RAM of USBDMA

Address	Bit	Name	Function	1	0	SR	R/W
0x18D6	D1						
USBDMA Register	D0	RAMAD[8]	Address for CPU read or write RAM of USBDMA	High	Low	0	R/W

D0 : Address for CPU read or write RAM of USBDMA

Address	Bit	Name	Function	1	0	SR	R/W
0x18D8	D2	SEND	Trigger cpu read or write RAM of USBDMA	Send	None	0	R/W
USBDMA Register	D1	WR1_RD0	Select read or write RAM	Write	Read	0	R/W
	D0	A0_B1	Select RAM A or RAM B	RAM B	RAM A	0	R/W

D2 : 1: Trigger cpu read or write RAM of USBDMA, 0: None

D1 : 1: CPU write RAM, 0: CPU read RAM

D0 : 1: Select RAM A, 0: Select RAM B

5.19 ADC System and Interrupt Status Registers

Address	Bit	Name	Function	1	0	SR	R/W
0x18E0 ADC Register	D7						
	D6	ADCMODE	Select operating mode	One shot	Normal	0	R/W
	D5	ADSEL1	ADC channel select	00 : AD0 01 : AD1	10 : AD2 11 : AD3	0	R/W
	D4	ADSEL0				0	R/W
	D3	ADCSH	Turn on ADC using one shot	on	off	0	R/W
	D2	IADC	ADC interrupt	R Yes W Reset	R No W None	0	Yes Reset
	D1	EIADC	ADC interrupt mask	enable	mask	0	R/W
	D0	ADCON	ADC on/off	on	off	0	R/W
0x18E2 ADC Register	D7	VALID	When VALID=0, ADC data is invalid and CPU should stop to read adc data	VALID	INVALID	0	R
	D6						
	D5	CHANNEL 1	ADC channel	00 : AD0 01 : AD1	10 : AD2 11 : AD3	0	R
	D4	CHANNEL 0				0	R
	D3	ADC11	ADC output data(From buffer)	high	low	0	R
	D2	ADC10		high	low	0	R
	D1	ADC9		high	low	0	R
	D0	ADC8		high	low	0	R
0x18E3 ADC Register	D7	ADC7		high	low	0	R
	D6	ADC6		high	low	0	R
	D5	ADC5		high	low	0	R
	D4	ADC4		high	low	0	R
	D3	ADC3		high	low	0	R
	D2	ADC2		high	low	0	R
	D1	ADC1		high	low	0	R
	D0	ADC0		high	low	0	R
0x18E4 ADC Register	D7	MAX7	MAX ADC value	high	low	0	R/W
	D6	MAX6		high	low	0	R/W
	D5	MAX5		high	low	0	R/W
	D4	MAX4		high	low	0	R/W
	D3	MAX3		high	low	0	R/W
	D2	MAX2		high	low	0	R/W
	D1	MAX1		high	low	0	R/W
	D0	MAX0		high	low	0	R/W

Address	Bit	Name	Function	1	0	SR	R/W
0x18E5 ADC Register	D7						
	D6						
	D5	XADCSH	Read ADC trigger signal	none	trigger	0	R
	D4	ADCCLK	Read ADC operation CLK	high	low	0	R
	D3	XADINT	Read ADC interrupt	none	interrupt	0	R
	D2	BUSY	ADC busy	Busy	none	0	R
0x18E6 ADC Register	D7	ADC11	ADC input data(From ADC)	high	low	0	R
	D6	ADC10		high	low	0	R
	D5	ADC9		high	low	0	R
	D4	ADC8		high	low	0	R
	D3	ADC7		high	low	0	R
	D2	ADC6		high	low	0	R
	D1	ADC5		high	low	0	R
	D0	ADC4		high	low	0	R
0x18E7 ADC Register	D7	ADC3	ADC input data(From ADC)	high	low	0	R
	D6	ADC2		high	low	0	R
	D5	ADC1		high	low	0	R
	D4	ADC0		high	low	0	R
	D3						
0x18E8 ADC Register	D7	PREDIV7	ADC system & MP3 clock pre-divider (ADC clock = Fosc3/(PREDIV+1))	high	low	0	R/W
	D6	PREDIV6		high	low	0	R/W
	D5	PREDIV5		high	low	0	R/W
	D4	PREDIV4		high	low	0	R/W
	D3	PREDIV3		high	low	0	R/W
	D2	PREDIV2		high	low	1	R/W
	D1	PREDIV1		high	low	1	R/W
	D0	PREDIV0		high	low	0	R/W
0x18E9 ADC Register	D7	POSTDIV7	ADC system & MP3 clock post-divider (sample rate) (sample-rate=clock/(POSTDIV+1))	high	low	0	R/W
	D6	POSTDIV6		high	low	0	R/W
	D5	POSTDIV5		high	low	0	R/W
	D4	POSTDIV4		high	low	1	R/W
	D3	POSTDIV3		high	low	1	R/W
	D2	POSTDIV2		high	low	1	R/W
	D1	POSTDIV1		high	low	1	R/W
	D0	POSTDIV0		high	low	1	R/W

5.19.1 ADC PROGRAM FLOW

1. **Set the register 0x18E8 to define the system clock of ADC.**
   System clock = Fosc3/(PREDIV+1)
   Set the register 0x18E9 to define the sample rate of ADC.
   Sample Rate = System clock/(POSTDIV+1)
2. **The hardware channels (AD0, AD1, AD2, AD3) are assigned by ADSEL0 & ADSEL1**
3. **The operating mode set to Normal or One Shot mode (18E0, D6)**
4. **When recording, ADCON=1 (the recording start). if ADCON=0, then recording stop**
5. **When IADC=1, 6502 read 18E2 & 18E3(the 12-bit ADC will generate 0-4095 digital output)**
6. **The 12-bit ADC output: 111111111111 -> 3.30 V**
   10000000000 -> 1.65 V
   00000000000 -> 0.00 V
   (the 12-bit ADC will generate 0-4095 digital output)
7. **The ADC system will automatically generate interrupt at every 8K or 16K sample**
8. **When CPU read 18E2 & 18E3, CPU should check VALID is 1 or 0.**
   IF VALID=0, this ADC data is invalid and CPU should stop to read 18E2 & 18E3, else if VALID=1, this ADC data is valid and CPU should keep going to read 18E2 & 18E3
9. **CPU should read 18E2 first, then 18E3**
10. **There are 32*16 buffer to prevent CPU missing IADC=1**
11. **CPU can get the biggest ADC[11:4] value from 18E4**
12. **18E5(D5, D4 & D3), 18E6 & 18E7 are for testing**

5.20 UART INTERFACE

The MA8201-H72 incorporates one half duplex UART interface that allow the asynchronous system. When the asynchronous system is selected, 8-bit data or 9-bit data transfer possible. The user can select the baud rate by the formula as description (Baud Rate = CpuClk/12, CpuClk/(8xBRSEL), CpuClk/16, CpuClk/(8xBRSEL)).

Address	Bit	Name	Function	1	0	SR	R/W
0x1834 UART	D7	TBRD7	Transmit/Received Buffer Registers TBR[7:0]	High	Low	0	R/W
	D6	TBRD6		High	Low	0	R/W
	D5	TBRD5		High	Low	0	R/W
	D4	TBRD4		High	Low	0	R/W
	D3	TBRD3		High	Low	0	R/W
	D2	TBRD2		High	Low	0	R/W
	D1	TBRD1		High	Low	0	R/W
	D0	TBRD0		High	Low	0	R/W

D[7:0] : UART transmit/receive data D7-D0

Address	Bit	Name	Function	1	0	SR	R/W
0x1835 UART	D7	SM00	Operating Mode	00 : 8 bit UART (CpuClk/12) 01 : 8 bit UART (Variable Rate) 10: 9 bit UART (CpuClk/16) 11 : 9 bit UART (Variable Rate)		01	R/W
	D6	SM01					
	D5						
	D4	REN	Enable Receive data (this bit will be clear to 0 after receive interrupt)	Enable Trigger	Disable	0	R/W
	D3	TB08	The 9th transmitted data bit	High	Low	0	R/W
	D2	RB08	The 9th received data bit	High	Low	0	R
	D1	TXINT	Transmit interrupt flag	R Yes W Reset	R No W None	0	R/W
	D0	RXINT	Receive interrupt flag	R Yes W Reset	R No W None	0	R/W

D[7:6] : Operation mode select, 00 : 8-bit synchronous UART(CpuClk/12) ; 01 : 8-bit asynchronous UART ; 10 : 9-bit synchronous UART(CpuClk/16) ; 11 : 9-bit asynchronous UART

D4 : Enable receive data, 0 : Disable ; 1 : Enable to trigger the receive data (this bit will be clear to 0 after receiving data)

D3 : Set the 9th transmitted data

D2 : Get the 9th received data

D1 : Transmit interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D0 : Receive interrupt factor flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

Address	Bit	Name	Function	1	0	SR	R/W
0x1836 UART	D7						
	D6						
	D5						
	D4						
	D3						
	D2						
	D1	ENTXINT	Enable Transmit Interrupt	Enable	Disable	0	R/W
	D0	ENRXINT	Enable Receive Interrupt	Enable	Disable	0	R/W

D1 : Transmit interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

D0 : Receive interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

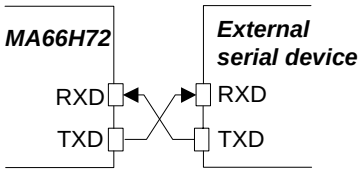
Address	Bit	Name	Function	1	0	SR	R/W
0x1837 UART	D7	UPreDIV7	UART clock pre-divider UART clock = CpuClk / (UPreDIV+1)*(UPostDIV+1)	high	low	0	R/W
	D6	UPreDIV6		high	low	0	R/W
	D5	UPreDIV5		high	low	0	R/W
	D4	UPreDIV4		high	low	0	R/W
	D3	UPreDIV3		high	low	0	R/W
	D2	UPreDIV2		high	low	0	R/W
	D1	UPreDIV1		high	low	0	R/W
	D0	UPreDIV0		high	low	0	R/W
0x1838 UART	D7	UPostDIV7	UART clock post-divider UART clock = CpuClk / (UPreDIV+1)*(UPostDIV+1)	high	low	0	R/W
	D6	UPostDIV6		high	low	0	R/W
	D5	UPostDIV5		high	low	0	R/W
	D4	UPostDIV4		high	low	0	R/W
	D3	UPostDIV3		high	low	0	R/W
	D2	UPostDIV2		high	low	0	R/W
	D1	UPostDIV1		high	low	0	R/W
	D0	UPostDIV0		high	low	0	R/W

UART clock divider : UART clock = CpuClk / (UPreDIV+1)*(UPostDIV+1)

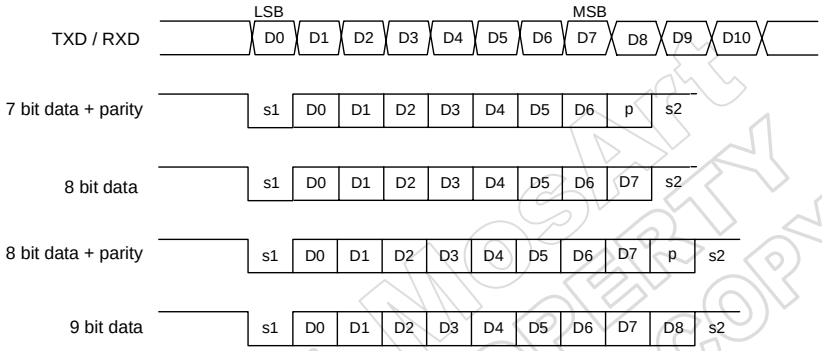
5.20.1 TRANSFER MODE

Asynchronous 8-bit/9-bit mode:

In this mode, as asynchronous 8-bit/9-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 8bits/9bits with or without parity. The hardware connects and timing as follow:



s1 : Start bit (1 bit)
s0 : Stop bit (1 bit)
p : Parity bit (1 bit)



5.20.2 DATA TRANSMIT PROCESS

The Control procedure and operation during transmitting is as follows.

1. Enable the Transmit Interrupt (ENTXINT).
2. Select the Operating Mode & Baud Rate.
3. Disable the Receive Status → Write "0" to REN.
4. Write the transmitting data into TB08 (if select 9 bit mode), then TRBRD7-TRBRD0.
5. Waiting the transmit interrupt, then clear the interrupt factor flag.
6. Repeat step 4 to 5 for the number of bytes of transmitting data, then transmitting is completed.

5.20.3 DATA RECEIVE PROCESS

The Control procedure and operation during receiving is as follows.

1. Enable the Receive Interrupt (ENRXINT).
2. Select the Operating Mode & Baud Rate.
3. Enable the Receive Status → Write "1" to REN.
4. Waiting the transmit interrupt, then read the receiving data from RB08 (if select 9 bit mode), then TRBRD7-TRBRD0.
5. Clear the interrupt factor flag.
6. Repeat step 3 to 5 for the number of bytes of receiving data, then receiving is completed.

5.21 CODEC DECODE

The MA8201-H72 has MPEG1/2 layer-III decoder. The decode can decode with MP3, PCM, ADPCM. There is one data buffer for storing the data of CODEC. If the buffer will be empty or full, the interrupt will be occurs. For the PCM and ADPCM, the decode provides encode and decode function with 8K, 16K, and 32K sample rate. The decode support ten Bands Equalizer with 64 steps for –20 to 20 dB gain. The decode support the thirty-two steps volume control also.

Address	Bit	Name	Function	1	0	SR	R/W
0x18F0 CODEC	D7	MP3DEC_SR	MP3 decoder reset	Reset	None	0	R/W
	D6	PCMDBL	PCM double sample rate	Enable	Disable	0	R/W
	D5	RSTBP	Reset R/W Buffer Pointer	Reset	None		W
	D4	MODE3	CODEC mode select	0000 : MP3 0001 : ADPCM Decoder 0010 : ADPCM Encoder 0011 : PCM		0000	R/W
	D3	MODE2					
	D2	MODE1					
	D1	MODE0					
	D0	ENCODE TRG	Encode trigger	Trigger	None	0	R/W

D7 : MP3 decoder reset, 0 = none, 1 = reset

D6 : set PCM double sample rate, 0 = Disable, 1 = Enable

D5 : Reset the Read/Write Buffer Pointer, 0 = None, 1 = Reset

D[4:1] : Mode select, 0000 = MP3, 0001 = ADPCM Decoder, 0010 = ADPCM Encoder, 0011 = PCM

D0 : Enable CODEC decode, 0 = Disable, 1 = Enable

Address	Bit	Name	Function	1	0	SR	R/W
0x18F3 CODEC	D7	RBFD7	Read Buffer	High	Low	0	R/W
	D6	RBFD6		High	Low	0	R/W
	D5	RBFD5		High	Low	0	R/W
	D4	RBFD4		High	Low	0	R/W
	D3	RBFD3		High	Low	0	R/W
	D2	RBFD2		High	Low	0	R/W
	D1	RBFD1		High	Low	0	R/W
	D0	RBFD0		High	Low	0	R/W

D[7:0] : Read data from buffer

Address	Bit	Name	Function	1	0	SR	R/W
0x18F1 CODEC	D7	WBFD7	Write Buffer (High Byte)	High	Low	0	R/W
	D6	WBFD6		High	Low	0	R/W
	D5	WBFD5		High	Low	0	R/W
	D4	WBFD4		High	Low	0	R/W
	D3	WBFD3		High	Low	0	R/W
	D2	WBFD2		High	Low	0	R/W
	D1	WBFD1		High	Low	0	R/W
	D0	WBFD0		High	Low	0	R/W
0x18F2 CODEC	D7	WBFD15	Write Buffer (Low Byte)	High	Low	0	R/W
	D6	WBFD14		High	Low	0	R/W
	D5	WBFD13		High	Low	0	R/W
	D4	WBFD12		High	Low	0	R/W
	D3	WBFD11		High	Low	0	R/W
	D2	WBFD10		High	Low	0	R/W
	D1	WBFD9		High	Low	0	R/W
	D0	WBFD8		High	Low	0	R/W

D[7:0] : Write data to buffer

Address	Bit	Name	Function	1		0		SR	R/W
0x18F4 CODEC	D7	BLKINT	ADPCM block finish flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D6	BUFWINT	CODEC buffer block write finish flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D5	BUFRINT	CODEC buffer block read finish flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D4	BUFRDY	CODEC buffer ready flag	Ready		Not Ready		1	R
	D3	EIBLK	ADPCM block finish interrupt mask register	enable		mask		0	R/W
	D2	EIBUFW	CODEC buffer block write finish interrupt mask register	enable		mask		0	R/W
	D1	EIBUFR	CODEC buffer block read finish interrupt mask register	enable		mask		0	R/W
	D0	ENREADY	Enable CODEC buffer ready signal	enable		disable		0	R/W

D7 : ADPCM block finish flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D6 : CODEC buffer block write finish flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D5 : CODEC buffer block read finish flag, read 0 = no interrupt, 1 = interrupt, write 0 = none, 1 = reset

D4 : indicate CODEC buffer ready signal, 0 = not ready, 1 = ready

D3 : ADPCM block finish interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

D2 : CODEC buffer block write finish interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

D1 : CODEC buffer block read finish interrupt mask register, 0 = enable interrupt, 1 = disable interrupt

D0 : Enable CODEC buffer ready signal, 0 = enable signal, 1 = disable signal

Address	Bit	Name	Function	1	0	SR	R/W
0x18F5 CODEC	D7	BLK1	Set Block A,B length Block Length = 2^(BKL+6) BKL = 0~3 (maximum 512 bytes)	High	Low	0	R/W
	D6	BLK0		High	Low	0	R/W
	D5	VOL5	CODEC Volume level select (22db, 21.5db, 21db, 20db, 19.5db, 18.8db, 18db, 17db, 16.6db, 16db, 15db, 14.5db, 14db, 13db, 12db, 11.6db, 11db, 10db, 9.4db, 8.7db, 8db, 7db, 6.5db, 6db, 5db, 4db, 3.6db, 3db, 2db, 1.4db, 0.7db, 0db, -1.4db, -3db, -4db, -5.5db, -7db, -8db, -9.6db, -11db, -12db, -14db, -15db, -16db, -18db, -19db, -21db, -22db, -23db, -25db, -26db, -28db, -29db, -30db, -32db, -33db, -34db, -36db, -37db, -39db, -40db, -41db, -42db, -44db)	High	Low	0	R/W
	D4	VOL4		High	Low	0	R/W
	D3	VOL3		High	Low	0	R/W
	D2	VOL2		High	Low	0	R/W
	D1	VOL1		High	Low	0	R/W
	D0	VOL0		High	Low	0	R/W

D[7:6] : Set the buffer length, Block length = 2^(BKL+6), BLK = 0~3

D[5:0] : Select Volume level, 0~63 steps **(22db, 21.5db, 21db, 20db, 19.5db, 18.8db, 18db, 17db, 16.6db, 16db, 15db, 14.5db, 14db, 13db, 12db, 11.6db, 11db, 10db, 9.4db, 8.7db, 8db, 7db, 6.5db, 6db, 5db, 4db, 3.6db, 3db, 2db, 1.4db, 0.7db, 0db, -1.4db, -3db, -4db, -5.5db, -7db, -8db, -9.6db, -11db, -12db, -14db, -15db, -16db, -18db, -19db, -21db, -22db, -23db, -25db, -26db, -28db, -29db, -30db, -32db, -33db, -34db, -36db, -37db, -39db, -40db, -41db, -42db, -44db)**

Address	Bit	Name	Function	1	0	SR	R/W
0x18F6 CODEC	D7	STEREO	Enable stereo mode	Stereo	Mono	0	R/W
	D6	TRGEQ	Trigger CODEC to using new band equalizer value	New	Old		W
	D5	B60HZ5	CODEC 60Hz band equalizer coefficients	High	Low	0	R/W
	D4	B60HZ4		High	Low	0	R/W
	D3	B60HZ3		High	Low	0	R/W
	D2	B60HZ2		High	Low	0	R/W
	D1	B60HZ1		High	Low	0	R/W
	D0	B60HZ0		High	Low	0	R/W

D7 : Turn on stereo mode, 0 = mono mode, 1 = stereo mode

D6 : Trigger CODEC decode to using new band equalizer value, 0 = old, 1 = new, write only

D[5:0] : Select 60Hz band equalizer coefficients, 0~63 steps

Address	Bit	Name	Function	1		0		SR	R/W
0x18F7 CODEC	D7	PCMBFOV	PCM buffer overrun flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D6	MP3BFOV	MP3 buffer overrun flag	R	Yes	R	No	0	R/W
				W	Reset	W	None		
	D5	B170HZ5	CODEC 170Hz band equalizer coefficients	High		Low		0	R/W
	D4	B170HZ4		High		Low		0	R/W
	D3	B170HZ3		High		Low		0	R/W
	D2	B170HZ2		High		Low		0	R/W
	D1	B170HZ1		High		Low		0	R/W
	D0	B170HZ0		High		Low		0	R/W

D7 : indicate the PCM buffer overrun status, read 0 = no overrun, 1 = overrun, write 0 = none, 1 = reset

D6 : indicate the MP3 buffer overrun status, read 0 = no overrun, 1 = overrun, write 0 = none, 1 = reset

D[5:0] : Select 170Hz band equalizer coefficients, 0~63 steps

Address	Bit	Name	Function	1	0	SR	R/W
0x18F8 CODEC	D7	PCMFULL	PCM FIFO full	Full	No full	0	R
	D6	PCM EMPTY	PCM FIFO empty	Empty	No empty	1	R
	D5	B310HZ5	CODEC 310Hz band equalizer coefficients	High	Low	0	R/W
	D4	B310HZ4		High	Low	0	R/W
	D3	B310HZ3		High	Low	0	R/W
	D2	B310HZ2		High	Low	0	R/W
	D1	B310HZ1		High	Low	0	R/W
	D0	B310HZ0		High	Low	0	R/W

D7 : indicate the PCM FIFO full status, 0 = no full, 1 = full, read only

D6 : indicate the PCM FIFO empty status, 0 = no empty, 1 = empty, read only

D[5:0] : Select 310Hz band equalizer coefficients, 0~63 steps

Address	Bit	Name	Function	1	0	SR	R/W
0x18F9 CODEC	D7	MP3FULL	MP3 FIFO full	Full	No full	0	R
	D6	MP3 EMPTY	MP3 FIFO empty	Empty	No empty	1	R
	D5	B600HZ5	CODEC 600Hz band equalizer coefficients	High	Low	0	R/W
	D4	B600HZ4		High	Low	0	R/W
	D3	B600HZ3		High	Low	0	R/W
	D2	B600HZ2		High	Low	0	R/W
	D1	B600HZ1		High	Low	0	R/W
	D0	B600HZ0		High	Low	0	R/W

D7 : indicate the MP3 FIFO full status, 0 = no full, 1 = full, read only

D6 : indicate the MP3 FIFO empty status, 0 = no empty, 1 = empty, read only

D[5:0] : Select 600Hz band equalizer coefficients, 0~63 steps

Address	Bit	Name	Function	1	0	SR	R/W
0x18FA CODEC	D5	B1KHZ5	CODEC 1KHz band equalizer coefficients	High	Low	0	R/W
	D4	B1KHZ4		High	Low	0	R/W
	D3	B1KHZ3		High	Low	0	R/W
	D2	B1KHZ2		High	Low	0	R/W
	D1	B1KHZ1		High	Low	0	R/W
	D0	B1KHZ0		High	Low	0	R/W

D[5:0] : Select 1KHz band equalizer coefficients, 0~63 steps

Address	Bit	Name	Function	1	0	SR	R/W
0x18FB CODEC	D5	B3KHZ5	CODEC 3KHz band equalizer coefficients	High	Low	0	R/W
	D4	B3KHZ4		High	Low	0	R/W
	D3	B3KHZ3		High	Low	0	R/W
	D2	B3KHZ2		High	Low	0	R/W
	D1	B3KHZ1		High	Low	0	R/W
	D0	B3KHZ0		High	Low	0	R/W

D[5:0] : Select 3KHz band equalizer coefficients, 0~63 steps

Address	Bit	Name	Function	1	0	SR	R/W
0x18FC CODEC	D5	B6KHZ5	CODEC 6KHz band equalizer coefficients	High	Low	0	R/W
	D4	B6KHZ4		High	Low	0	R/W
	D3	B6KHZ3		High	Low	0	R/W
	D2	B6KHZ2		High	Low	0	R/W
	D1	B6KHZ1		High	Low	0	R/W
	D0	B6KHZ0		High	Low	0	R/W

D[5:0] : Select 6KHz band equalizer coefficients, 0~63 steps

Address	Bit	Name	Function	1	0	SR	R/W
0x18FD CODEC	D5	B12KHZ5	CODEC 12KHz band equalizer coefficients	High	Low	0	R/W
	D4	B12KHZ4		High	Low	0	R/W
	D3	B12KHZ3		High	Low	0	R/W
	D2	B12KHZ2		High	Low	0	R/W
	D1	B12KHZ1		High	Low	0	R/W
	D0	B12KHZ0		High	Low	0	R/W

D[5:0] : Select 12KHz band equalizer coefficients, 0~63 steps

Address	Bit	Name	Function	1	0	SR	R/W
0x18FE CODEC	D5	B14KHZ5	CODEC 14KHz band equalizer coefficients	High	Low	0	R/W
	D4	B14KHZ4		High	Low	0	R/W
	D3	B14KHZ3		High	Low	0	R/W
	D2	B14KHZ2		High	Low	0	R/W
	D1	B14KHZ1		High	Low	0	R/W
	D0	B14KHZ0		High	Low	0	R/W

D[5:0] : Select 14KHz band equalizer coefficients, 0~63 steps

Address	Bit	Name	Function	1	0	SR	R/W
0x18FF CODEC	D5	B16KHZ5	CODEC 16KHz band equalizer coefficients	High	Low	0	R/W
	D4	B16KHZ4		High	Low	0	R/W
	D3	B16KHZ3		High	Low	0	R/W
	D2	B16KHZ2		High	Low	0	R/W
	D1	B16KHZ1		High	Low	0	R/W
	D0	B16KHZ0		High	Low	0	R/W

D[5:0] : Select 16KHz band equalizer coefficients, 0~63 steps

6. DC/AC & ADC & USB CHARACTER

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power supply						
Vdd	Supply voltage		2.5	3.0	3.6	V
Iss	Operation current (3.0V)	Osc = 32 kHz		3		mA
Iss	Operation current (3.0V)	Osc = 12 MHz (PLL)		10		mA
Iss	Operation current (3.0V)	Osc = 48 MHz		25		mA
Current consumption for MP3 playing						
Iss	Operation current (3.0V)	Osc = 12 MHz (PLL)		17		mA
Iss	Operation current (3.0V)	Osc = 48 MHz		32		mA
Input						
V_{IH}	high level input voltage		1.0			Vdd
V_{IL}	low level input voltage				0.6	Vdd
I_{IH}	high level input voltage	vdd=3.3v, vin=3.3v	0		0.5	uA
I_{IL}	low level input voltage	vdd=3.3v, vin=0v	-0.5		0	uA
Output						
I_{OL}	low level output current	vdd=3.3v, vout=0.6v		10		mA
I_{OH}	high level output current	vdd=3.3v, vout=2.7v		10		mA
Temperature						
Ambient Operating Temperature (power applied)			-20		80	^{0}C
Storage Temperature			-65		150	^{0}C
ADC characteristics						
Vdd	Supply voltage		2.5	3.0	3.6	V
	Resolution	Vdd=3.0v		11		Bits
Fs	Maximum conversion time	Vdd=3.0v	1.0			MHz
DNL	Differential Nonlinearity	Vdd=3.0v			1.0	LSB
INL	Integral Nonlinearity	Vdd=3.0v			0.8	LSB

Results based on USB-IF / Waiver Limits :

Measurement Name	Minimum	Maximum	Mean	pk-pk	Standard Deviation	RMS	Status
Eye Diagram Test	-	-	-	-	-	-	Pass
Signal Rate	11.85856Mbps	12.19512Mbps	11.99641Mbps	0.0000bps	131.8621kbps	12.00923Mbps	Pass
Crossover Voltage	1.617143 V	1.720000 V	1.666776 V	102.8571mV	39.23932mV	1.667196 V	Pass
EOP Width	-	-	165.3344ns	-	-	-	Pass
Consecutive Jitter	-885.3928ps	538.7830ps	0.0000s	1.424176ns	524.4194ps	500.0143ps	Pass
Paired JK Jitter	-167.0330ps	145.0549ps	0.0000s	312.0879ps	126.4453ps	113.0961ps	Pass
Paired KJ Jitter	-265.2747ps	574.7253ps	113.7862ps	840.0000ps	352.8428ps	326.0688ps	Pass